Statistical Gate Delay Model for Multiple Input Switching

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Abstract— In this paper, we propose a calculation method of gate delay for SSTA (Statistical Static Timing Analysis) considering MIS (Multiple Input Switching). Most SSTA approaches assume a single input switching model and ignore the effect of MIS on gate delay. MIS occurs when multiple inputs of a gate switch nearly simultaneously. Thus, ignoring MIS causes error in MAX operation in SSTA. We propose a statistical gate delay model considering MIS. We verify the proposed method by SPICE based Monte Carlo simulations and experimental results show that the proposed method improves the error due to ignoring MIS.

I. Introduction

Process scaling makes it possible to improve circuit performance. On the other hands, the impact of process variations on performance has been increasing. In such a situation, STA (Static Timing Analysis) is no longer able to capture the circuit performance accurately. In STA, the best/worst corners are used to capture the circuit performance. The corner based analysis is valid when die-to-die variation is dominant. However, in recent processes, within-die variation has been becoming significant. In such a situation, the timing prediction by the corner based analysis becomes too pessimistic. Therefore, SSTA (Statistical Static Timing Analysis) has been developed to consider the statistical characteristics of timing issue.

Canonical delay model is widely used in a lot of SSTA approaches [1–4]. This model considers delays and transition times as functions of process parameters, and can handle spatial correlations efficiently. Reference [1, 2] use a first-order canonical delay model, which assumes that all the variations are expressed by normal distributions. While, higher order delay models have studied in [3,4] to handle non normal distributions. In SSTA, one of the error sources is the statistical maximum operation because the result of maximum of two normal distributions is a skewed non normal distribution. Some researchers have discussed the computation of the statistical maximum operation [4, 5]. However, other sources of errors exist in simultaneous switching such as MIS (Multiple Input Switching) [6–9]. When multiple inputs of a gate switch simultaneously or close to each other, the gate delay can increase or decrease compared to that of SIS (Single Input Switching). Therefore, the effect of MIS should be discussed for accurate timing analysis. Several researchers have discussed the effect of MIS in STA [6, 7] and SSTA [8, 9]. However, it is not clear whether these methods could be applicable to canonical delay models.

In this paper, we propose a gate delay model that can be applied to the first-order canonical delay model. The proposed model modifies the gate delay by the timing difference between the transitions of inputs to handle the effect of MIS on the gate delays. The proposed method can also handle the effect of input transition variations on the delay.

This paper also discusses the distribution in output transition times. The distribution in output transition times affects the result of SSTA. However, in even a conventional SSTA that does not consider MIS, the treatment of output transition times of a multiple input gate has not been investigated in details, with a few exceptions [1, 2]. Furthermore, MIS affects output transition times as well as gate delays. We propose a calculation method of gate delay and output transition time considering MIS. We compare the result by the proposed method to that by Monte Carlo analysis of a transistor level simulation. Results show that the proposed method improves the error due to ignoring MIS.

The rest of this paper is organized as follows. Section II shows the effect of MIS on the gate delay and output transition time. Section III proposes a gate delay model considering MIS. Section IV verifies the proposed method by the Monte Carlo analysis of a transistor level simulation. Section V concludes this paper.

II. Effect of Multiple Input Switching

In SSTA, the statistical maximum operation is necessary to estimate the output distribution of a gate with multiple inputs. Fig. 1 shows an example of the statistical maximum operation in a 2-input NAND gate. The output arrival time A_{OUT} is calculated as $\mathrm{MAX}(A_{\mathrm{A}} + D_{\mathrm{A}}, A_{\mathrm{B}} + D_{\mathrm{B}})$ where A is the arrival time and D is the gate delay from the input to the output. The subscripts A and B correspond to the inputs A and B. Typically, SSTA characterizes the gate delay from each input to output under a single input switching (SIS), which assumes that only one of the inputs switches. However, when the multiple inputs switch simultaneously, the gate delay changes. For example, as inputs A and B rise simultaneously, the two p-channel transistors that are connected in parallel start to conduct simultaneously and the delay becomes small. On the other hands, as inputs A and B fall simultaneously, the delay becomes large. Thus in the case of simultaneous switching, SIS assumption is not accurate and it is necessary to consider the effect of MIS.

We show the effect of MIS on gate delay and output transition time by a transistor level simulation [10]. We use a 2-input

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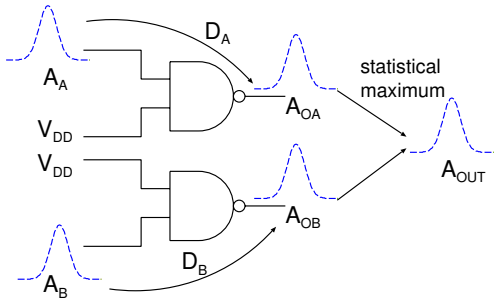

Fig. 1. Example of the statistical maximum operation in SSTA

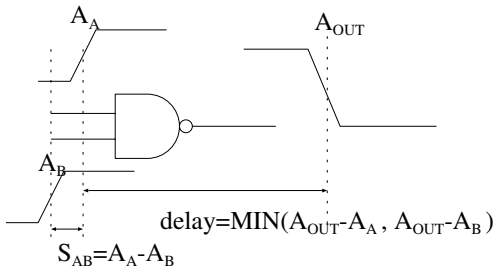

Fig. 2. Gate delay of falling output transition

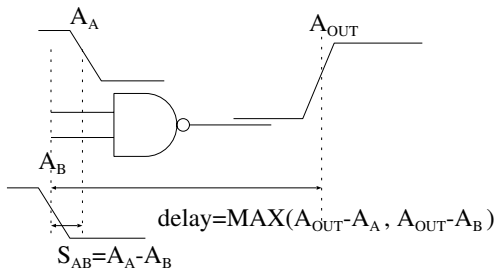

Fig. 3. Gate delay of rising output transition

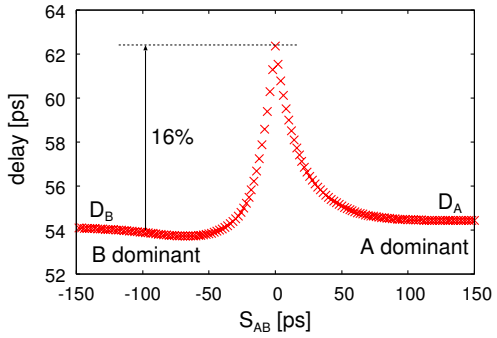

Fig. 4. Example of the gate delay of falling output transition

NAND gate in a 90nm CMOS process as an example. The gate delay can be classified into two cases, i.e. falling transition and rising transition. Fig. 2 shows falling output transition. The rising of both inputs A and B makes the output fall, thus the gate delay is defined as $\mathrm{MIN}(A_{\mathrm{OUT}} - A_{\mathrm{A}}, A_{\mathrm{OUT}} - A_{\mathrm{B}})$. Fig. 3 shows rising output transition. The falling of only one of the inputs A and B makes the output rise and the gate delay is defined as $\mathrm{MAX}(A_{\mathrm{out}} - A_{\mathrm{A}}, A_{\mathrm{OUT}} - A_{\mathrm{B}})$.

Fig. 4 and Fig. 5 show the results of the fall and rise delay as a function of the separation between inputs A and B ($S_{\mathrm{AB}} = A_{\mathrm{A}} - A_{\mathrm{B}}$), respectively. Fig. 6 shows the result of the output transition time in the case of the rising output transition. The output load is set to FO4 and transition times of inputs are set to $100\,\mathrm{ps}$. In Fig. 4, as the separation S_{AB} gets closer to 0, the gate delay increases by 16% in maximum. Under SIS assumption, D_{A} and D_{B} are $54.5\,\mathrm{ps}$ and $54.0\,\mathrm{ps}$, respectively. However, as seen in Fig. 4, realistic gate delays are much larger when two inputs switch nearly simultaneously. On the other hand, as shown in Fig. 5, as S_{AB} gets closer to 0, the gate delay decreases by 34% in maximum. These results indicate that the conventional SSTA that ignores MIS can underestimate or overestimate the gate delay. In addition, Fig. 6 indicates that the output transition time has the same tendency of the gate delay. In general, the effect of MIS on the delay tends to become a significant problem when the transistors that are connected in parallel conduct simultaneously. Thus, this case needs more attention to modeling.

From the discussion above, the effect of MIS on the delay becomes large when the separation S_{AB} gets close to 0. Therefore, in SSTA, it is necessary not only to consider the accuracy of the statistical maximum operation but also to handle the effect of MIS.

In real circuits, all the gates are not affected by MIS because there are many single input gates (inverters and buffers). The importance of considering MIS depends on kinds of circuits. It seems that the effect of MIS can be negligible in large circuits. However, according to [7], which evaluated the effect of MIS in ISCAS benchmark circuits [11], MIS can lead to an error in min-delay, which results in hold violation. This is because the min-delay depends on the shortest path of the circuit. Therefore, the effect of MIS should be considered in even large circuits.

III. Gate Delay Model for Multiple Input Switching

In this section, we propose a gate delay model for multiple input switching. Section III-A explains how the proposed method handles the effect of MIS on the gate delay. Section III-B shows that the proposed method can be applied to an existing gate delay model in SSTA. Section III-C discusses output transition times of multiple input gates.

A. Proposed Gate Delay Modeling

As mentioned in Section II, most conventional SSTA characterize the gate delays from each input to the output under SIS assumption, which overestimates or underestimates the gate delay in the case of simultaneously switching inputs. The proposed gate delay model considers each gate delay as a function of the separation between inputs A and B (S_{AB}) as shown

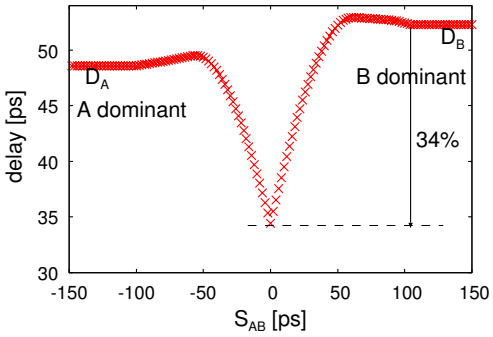

Fig. 5. Example of the gate delay of rising output transition

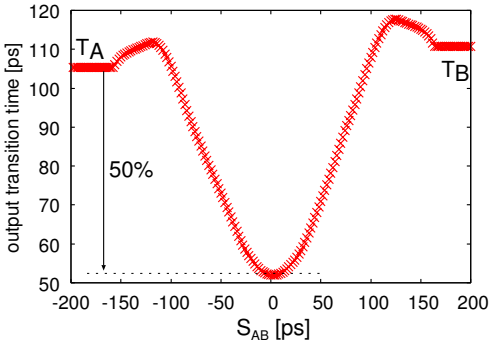

Fig. 6. Example of the output transition time of rising output transition

in Fig. 7. In other words, the proposed method modifies the each gate delay by the magnitude of MIS effect. The proposed model modifies only each gate delay and does not change other parts such as the distribution of input arrival times and so on. Therefore, the advantage of the proposed method is to be able to use the statistical maximum operation in conventional SSTA such as Clark's method [12].

Overview of the proposed gate delay modeling is described as below. We explain the calculation method of the proposed gate delay $D_{\rm A}(S_{\rm AB})$ and $D_{\rm B}(S_{\rm AB})$ by an example of a falling output transition in a 2-input NAND gate in Fig. 7.

Step 1. Estimate the value of the gate delay as a function of $S_{\rm AB}$ by transistor level simulation (SPICE), like Fig. 4.

Step 2. From the result of Step 1, calculate the delay from A to output and the delay from B to output as described later.

Step 3. From the each delay of Step 2, estimate the mean and variance of the each gate delay.

Fig. 8 shows the proposed calculation method of each gate delay. In a conventional method that does not consider MIS, the gate delay $D_{\rm A}$ and $D_{\rm B}$ are fixed values regardless of $S_{\rm AB}$. The proposed method considers $D_{\rm A}$ and $D_{\rm B}$ as a function of $S_{\rm AB}$ Therefore, it is necessary to find how $D_{\rm A}$ and $D_{\rm B}$ vary with $S_{\rm AB}$. However, we cannot estimate $D_{\rm A}$ and $D_{\rm B}$ individually at any $S_{\rm AB}$ from the result of Step 1 because we can know the only $\mathrm{MIN}(A_{\rm OUT} - A_{\rm A}, A_{\rm OUT} - A_{\rm B})$ by the results of

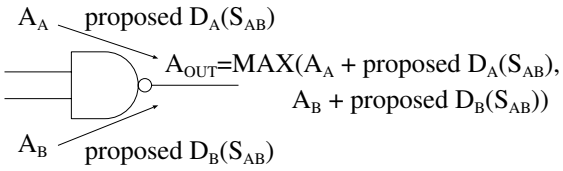

Fig. 7. Proposed gate delay model for MIS

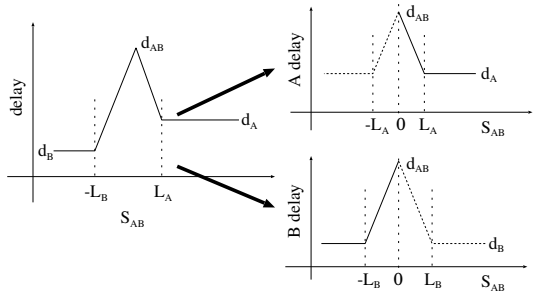

Fig. 8. Proposed calculation method of gate delay

SPICE. For example, $D_{\rm A}(S_{\rm AB})$ is equal to $A_{\rm OUT} - A_{\rm A}$ when $S_{\rm AB} > 0$ ($A_{\rm OUT} - A_{\rm A} < A_{\rm OUT} - A_{\rm B}$). When $S_{\rm AB} < 0$, $D_{\rm A}$ is not equal to $A_{\rm OUT} - A_{\rm A}$ because $A_{\rm OUT} - A_{\rm B}$ is smaller than $A_{\rm OUT} - A_{\rm A}$. Thus, we estimate $D_{\rm A}(S_{\rm AB})$ at any $S_{\rm AB}$ under the assumption shown in Fig. 8. In Fig. 8, $L_{\rm A}$ shows the border value of $S_{\rm AB}$ where the input B does not affect $D_{\rm A}$. In other words, $D_{\rm A}$ is equal to the gate delay $d_{\rm A}$ in SIS when $S_{\rm AB} > L_{\rm A}$. First, we assume that $D_{\rm A}(S_{\rm AB})$ is equal to the result of Step 1 when $S_{\rm AB} > 0$. Then, we assume that $D_{\rm A}(S_{\rm AB}) = D_{\rm A}(-S_{\rm AB})$ when $S_{\rm AB} < 0$, that is, $D_{\rm A}(S_{\rm AB})$ is symmetric with respect to $S_{\rm AB} = 0$. On the other hand, we assume that $D_{\rm B}(S_{\rm AB})$ is equal to the result of Step 1 when $S_{\rm AB} < 0$, and that $D_{\rm B}(S_{\rm AB}) = D_{\rm B}(-S_{\rm AB})$ when $S_{\rm AB} > 0$.

In this paper, we assume that delay variations are normally distributed, and thereby it is necessary to calculate the mean and variance of the gate delays estimated in Step 2. We define $\mu(D_{\rm A})$ and $\sigma^2(D_{\rm A})$ as the mean and the variance of $D_{\rm A}(S_{\rm AB})$, respectively. From the definition of the mean and the variance, $\mu(D_{\rm A})$ and $\sigma^2(D_{\rm A})$ are given by

$$\mu(D_{\rm A}) = \int_{-\infty}^{\infty} D_{\rm A}(S_{AB}) p(S_{AB}) {\rm d}S_{\rm AB} \qquad (1)$$

$$\sigma^2(D_{\rm A}) = \int_{-\infty}^{\infty} (D_{\rm A}(S_{AB}) - \mu(D_{\rm A}))^2 p(S_{AB}) {\rm d}S_{\rm AB} \qquad (2)$$

where $p(S_{\rm AB})$ is the probability density function of $S_{\rm AB}$. When $A_{\rm A}$ and $A_{\rm B}$ are normally distributed, $A_{\rm A} \sim N(\mu_{\rm A}, \sigma_{\rm A}^2)$, $A_{\rm B} \sim N(\mu_{\rm B}, \sigma_{\rm B}^2)$, with these correlation coefficient ρ_{AB}, $S_{\rm AB}$ is also normally distributed, $S_{\rm AB} \sim N(\mu_{\rm AB}, \sigma_{\rm AB}^2) \sim N(\mu_{\rm A} - \mu_{\rm B}, \sigma_{\rm A}^2 + \sigma_{\rm B}^2 - 2\rho_{\rm AB}\sigma_{\rm A}\sigma_{\rm B})$. Thus, $p(S_{\rm AB})$ is given by

$$p(S_{\rm AB}) = \frac{1}{\sqrt{2\pi}\sigma_{\rm AB}} \exp\left[-\frac{(S_{\rm AB} - \mu_{\rm AB})^2}{2\sigma_{\rm AB}^2}\right]. \qquad (3)$$

In addition, $D_{\rm A}$ correlates with $S_{\rm AB}$ because $D_{\rm A}$ varies with $S_{\rm AB}$. In order to consider this correlation, it is necessary to

calculate the covariance $\mathrm{Cov}(S_{\mathrm{AB}}, D_{\mathrm{A}})$ from the definition of the covariance. The covariance $\mathrm{Cov}(S_{\mathrm{AB}}, D_{\mathrm{A}})$ is given by

$$\mathrm{Cov}(S_{\mathrm{AB}}, D_{\mathrm{A}}) = \int_{-\infty}^{\infty} (S_{\mathrm{AB}} - \mu_{\mathrm{AB}})(D_{\mathrm{A}}(S_{\mathrm{AB}}) - \mu(D_{\mathrm{A}})) \, p(S_{\mathrm{AB}}) \mathrm{d}S_{\mathrm{AB}} \quad (4)$$

Similarly, $\mu(D_{\mathrm{B}})$ and $\sigma^2(D_{\mathrm{B}})$ can be calculated as Eq. (1) and Eq. (2).

B. Expression for Canonical Gate Delay Model

In SSTA, all the delays and arrival times are commonly represented in canonical delay model. This paper discusses the first-order canonical delay form because we assume that all the delays have normal distributions. The example of the first-order canonical delay form d_i is given by

$$d_i = \mu_i + \sum_{j=1}^{k} \alpha_{i,j} r_j \quad (5)$$

where μ_i is the mean value of d_i, r_j is a normally distributed random variable, $r_i \sim N(0,1)$ and $\alpha_{i,j}$ is the first order sensitivity of the delay with respect to r_j. The advantage of this model is to calculate the statistical plus and maximum operation with correlation effectively.

We discuss how to calculate the canonical delay model of the proposed gate delay. The proposed and conventional gate delays from the input A to the output are expressed as $D_{\mathrm{A}}^{\mathrm{new}}(= \mu_{\mathrm{A}}^{\mathrm{new}} + \sum_{j=1}^{k} \alpha_{\mathrm{A},j}^{\mathrm{new}} r_j)$, $D_{\mathrm{A}}^{\mathrm{old}}(= \mu_{\mathrm{A}}^{\mathrm{old}} + \sum_{j=1}^{k} \alpha_{\mathrm{A},j}^{\mathrm{old}} r_j)$, respectively. The canonical delay form of the conventional gate delay($D_{\mathrm{A}}^{\mathrm{old}}$) can express how input transition times and transistor parameters affect the delay. However, as shown in Section III-A, we need to add the effect of $S_{\mathrm{AB}}(= \mu_{\mathrm{S}} + \sum_{j=1}^{k} \alpha_{\mathrm{S},j} r_j)$ on the delay into the canonical model. In order to explain how to calculate $D_{\mathrm{A}}^{\mathrm{new}}$, we classify $D_{\mathrm{A}}^{\mathrm{new}}$ into three terms, $\mu_{\mathrm{A}}^{\mathrm{new}}$, $\Delta D_{\mathrm{S}}(= \sum_{j=1}^{k} \beta_j r_j)$, $\Delta D_{\mathrm{other}}(= \sum_{j=1}^{k} \gamma_j r_j)$. Here, ΔD_{S} shows the effect of S_{AB} on the delay, and $\Delta D_{\mathrm{other}}$ shows the effect of other factors, such as input transition times and transistor parameters, on the delay. These relations are satisfied by $D_{\mathrm{A}}^{\mathrm{new}} = \mu_{\mathrm{A}}^{\mathrm{new}} + \Delta D_{\mathrm{S}} + \Delta D_{\mathrm{other}}$.

First, we obtain $\mu_{\mathrm{A}}^{\mathrm{new}} = \mu(D_{\mathrm{A}})$ from Eq. (1). Then, we set $\beta_j = k\alpha_{\mathrm{S},j}$ from the fact that D_{A} correlates with S_{AB}. Substituting $\alpha_{A,j} = k\alpha_{S,j}$ into Eq. (2), we obtain $k^2 = \sigma^2(D_{\mathrm{A}})/\sigma^2(S_{\mathrm{AB}})$ where $\sigma^2(S_{\mathrm{AB}}) = \sum_{j=1}^{k} \alpha_{S,j}^2$. As far as the sign of k concerned, we assume $k > 0$ when $\mathrm{Cov}(S_{\mathrm{AB}}, D_{\mathrm{A}}) > 0$ and $k < 0$ when $\mathrm{Cov}(S_{\mathrm{AB}}, D_{\mathrm{A}}) < 0$. Put it all together, β_j is given by

$$\beta_j = \begin{cases} \frac{\sigma(D_{\mathrm{A}})}{\sigma(S_{\mathrm{AB}})}\alpha_{S,j} & (\mathrm{Cov}(S_{\mathrm{AB}}, D_{\mathrm{A}}) > 0) \\ -\frac{\sigma(D_{\mathrm{A}})}{\sigma(S_{\mathrm{AB}})}\alpha_{S,j} & (\mathrm{Cov}(S_{\mathrm{AB}}, D_{\mathrm{A}}) < 0) \end{cases} . \quad (6)$$

Finally, we calculate γ_j by modifying already known coefficients ($\alpha_{\mathrm{A},j}^{\mathrm{old}}$). We could obtain much more correct γ_j by simulating the sensitivity of the delay with respect to r_j in any S_{AB}. However, these simulations are very expensive. We set $\gamma_j = (\mu_{\mathrm{A}}^{\mathrm{new}}/\mu_{\mathrm{A}}^{\mathrm{old}})\alpha_{\mathrm{A},j}^{\mathrm{old}}$ from the assumption that the proportion of the delay variation to r_j is constant even if the mean of the delay changes from $\mu_{\mathrm{A}}^{\mathrm{old}}$ to $\mu_{\mathrm{A}}^{\mathrm{new}}$. The canonical form of $D_{\mathrm{B}}^{\mathrm{new}}$ can be calculated in a similar way.

C. Output Transition Time Considering Multiple Input Switching

In SSTA, the transition times should be also expressed by the statistical values. However, there are few studies on the treatment of the distributions of the output transition time. In [1], the output transition time is computed as a weighted sum of the output transition through each input, where the weight equals the probability that the path through the input is the longest in others. For example, in a two-input NAND gate as shown in Fig.7, the output transition time T_{OUT} is given by

$$T_{\mathrm{OUT}} = \mathrm{Prob}[(A_{\mathrm{A}} + D_{\mathrm{A}}) > (A_{\mathrm{B}} + D_{\mathrm{B}})] T_{\mathrm{OUT,A}} + \mathrm{Prob}[(A_{\mathrm{A}} + D_{\mathrm{A}}) < (A_{\mathrm{B}} + D_{\mathrm{B}})] T_{\mathrm{OUT,B}} \quad (7)$$

where $\mathrm{Prob}[(\mathrm{A_A} + \mathrm{D_A}) > (\mathrm{A_B} + \mathrm{D_B})]$ corresponds to the probability that $A_{\mathrm{A}} + D_{\mathrm{A}}$ is larger than $A_{\mathrm{B}} + D_{\mathrm{B}}$, and $T_{\mathrm{OUT,A}}$ and $T_{\mathrm{OUT,A}}$ correspond to the output transition time through input A and B, respectively. Although this idea is reasonable, it is not clear whether it is correct from the viewpoint of electrical properties. As mentioned in Section II, MIS affects transition times as well as gate delays. Therefore, we improve (7) to consider the effect of MIS. We use the proposed gate delays ($D_{\mathrm{A}}^{\mathrm{new}}, D_{\mathrm{B}}^{\mathrm{new}}$) instead of the conventional gate delays ($D_{\mathrm{A}}^{\mathrm{old}}, D_{\mathrm{B}}^{\mathrm{old}}$) in (7). In addition, we estimate $T_{\mathrm{OUT,A}}^{\mathrm{new}}$ and $T_{\mathrm{OUT,B}}^{\mathrm{new}}$ in a similar way of Section III-B. In next section, we compare the proposed method to the Monte Carlo analysis of transistor level simulations.

IV. SSTA Considering Multiple Input Switching

In this section, we show that the proposed method can handle the effect of MIS on the delay by comparing the proposed method to the Monte Carlo analysis of transistor level simulations (SPICE). First, we show the result with varying S_{AB} only. Then, we show the result with varying S_{AB}, gate length and input transition time.

A. Experimental Conditions

We use the SPICE based Monte Carlo simulations [10] as our golden model. We use a 2-input NAND shown in Fig. 1 and a set of 90nm process parameters. The input transition times are set to 50ps, 100ps, 200ps and 400ps, and the load capacitance is set to FO1, FO4 and FO16. We vary S_{AB} in ranges which corresponds to $-L_{\mathrm{B}} < S_{\mathrm{AB}} < L_{\mathrm{A}}$ in Fig. 8. For example, S_{AB} is set to $N(0\mathrm{ps}, 10\,\mathrm{ps})$, $N(10\mathrm{ps}, 10\,\mathrm{ps})$, $N(20\mathrm{ps}, 10\,\mathrm{ps})$ and so on. We evaluate the error in the mean (μ), the standard deviation (σ) and $\mu + 3\sigma$ of the gate delay distribution.

As mentioned in Section II, the calculation of the output arrival time A_{OUT} is different by falling output transition and rising output transition. In the falling output transition, the output arrival time A_{OUT} is given by $A_{\mathrm{OUT}} = \mathrm{MAX}(A_{\mathrm{A}} + D_{\mathrm{A}}, A_{\mathrm{B}} + D_{\mathrm{B}})$. In the rising output transition, the output arrival time A_{OUT} is given by $A_{\mathrm{OUT}} = \mathrm{MIN}(A_{\mathrm{A}} + D_{\mathrm{A}}, A_{\mathrm{B}} + D_{\mathrm{B}})$. We use the Clark's method [12], which is commonly used to calculate a maximum/minimum of two normal distributions in SSTA.

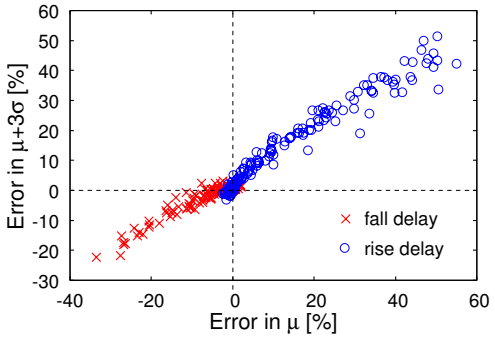

Fig. 9. Error in μ and $\mu + 3\sigma$ between the conventional method (w/o MIS) and SPICE based Monte Carlo simulations

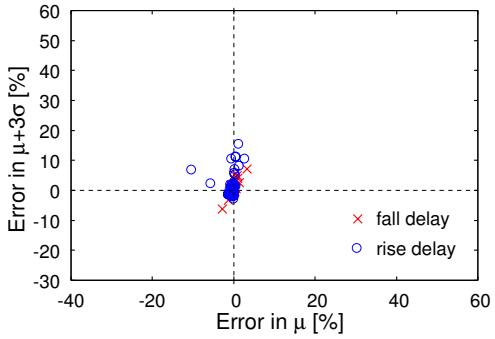

Fig. 10. Error in μ and $\mu + 3\sigma$ between the proposed method and SPICE based Monte Carlo simulations

B. Experimental Results

Fig. 9 shows the error in μ and $\mu + 3\sigma$ between the conventional method that does not consider MIS and SPICE based Monte Carlo simulations. Fig. 10 shows the error in μ and $\mu + 3\sigma$ between the proposed method and SPICE based Monte Carlo simulations. In figures, $\times$ and $\circ$ correspond to a result of a falling arrival time and rising arrival time, respectively.

From Fig. 9, we can see that the conventional method causes large error. The errors in μ are scattered between -30% and 60%. The case of the large errors in μ corresponds to the case where the distribution of S_{AB} varies around 0. The maximum error in $\mu + 3\sigma$ is also more than 50%. On the other hand, Fig. 10 shows that the result of the proposed method is close to Monte Carlo simulations. In the case of the proposed method, the maximum error in μ is 10% and that in $\mu + 3\sigma$ is 15%. These results indicate that the proposed method can consider MIS effect on gate delay.

Even if the proposed method is used, the error in $\mu + 3\sigma$ is more than 15% in some cases. These cases correspond to cases where S_{AB} varies around 0. The main causes of the error are the approximation error of the normal distribution and the estimation error of Clark's method. When the gate delay is a linear function of S_{AB}, the assumption of the normal distribution is valid. However, the gate delay is not linear to S_{AB} when S_{AB} varies around 0, as shown Fig.8. Therefore, the distribution of the gate delay is not normally distributed when the mean of S_{AB} is close to 0. The other reason is that the accuracy of the Clark's method becomes worse as the mean of S_{AB} gets closer to 0. This is because the maximum of two normal distributions is a skewed distribution when the means of these distributions are very close.

Table I shows the numerical example of the error between the proposed method and the conventional method when each input transition time are set to 100 ps and the output capacitance is set to FO4 and 3-sigma variation of S_{AB} is set to 28ps. The first column shows the mean of S_{AB}. From Table I, we can see that the error becomes larger as the distribution of S_{AB} gets closer to 0. Thus, the conventional method that does not consider MIS leads to significant inaccuracy when multiple inputs of a gate switch simultaneously. The proposed method improves the error by considering the effect of MIS.

TABLE I
EXAMPLE OF THE ERROR BETWEEN THE PROPOSED METHOD AND THE CONVENTIONAL METHOD (FO4)

Mean of S_{AB} [ps]	Proposed SSTA			SSTA (w/o MIS)		
	% error in μ	% error in σ	% error in $\mu + 3\sigma$	% error in μ	% error in σ	% error in $\mu + 3\sigma$
0	0.45	27.66	11.41	43.74	17.55	37.88
10	−0.71	5.91	1.57	34.11	22.95	33.34
20	−1.01	−0.71	−1.00	21.10	32.72	26.67
30	−0.76	−1.77	−1.14	10.84	28.18	17.17
40	−0.47	−1.71	−0.90	4.38	18.60	9.25
50	−0.23	−1.85	−0.78	0.93	9.13	3.71
60	−0.08	−1.57	−0.59	−0.48	2.89	0.63

C. Proposed Method under Variability in Input Transition Time and Gate Length

In real circuits, it is necessary to consider the variations of not only S_{AB} but also input transition time and transistor parameters (e.g. gate length). As mentioned in Section III, canonical delay model can handle the effect of these variations on gate delay by adding these corresponding terms. We compare SPICE based Monte Carlo simulations to the proposed method when S_{AB}, input transition time and gate length vary. Furthermore, we evaluate the distribution of the output transition time. In experiments, 3-sigma variations of the input transition time and gate length are set to 20%. In the case of Table I, when the gate length increases by 20%, the delay increases by about 30%, and when the input transition time increases by 20%, the delay increases by about 10%. Thus, these variations strongly affect the delay variations.

Figs. 11 and 12 show the results in the case of rising output transition. Fig. 11 shows the result of the conventional method and SPICE based Monte Carlo simulations. Fig. 12 shows the error in μ and $\mu + 3\sigma$ between the proposed method and SPICE based Monte Carlo simulations. In figures, $\circ$ and $\triangle$ correspond to a result of gate delay and output transition time, respectively. From the difference between Fig. 11 and Fig. 12, we can see that the proposed can improve the error due to ignoring MIS. The proposed method can estimate the distribution of the delay and output transition time under MIS conditions.

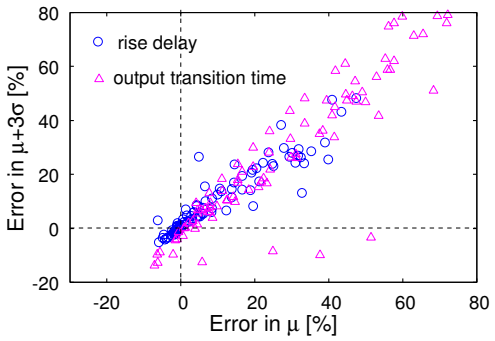

Fig. 11. Error in μ and $\mu + 3\sigma$ between the conventional method (w/o MIS) and SPICE based Monte Carlo simulations under the variability in S_{AB}, input transition and gate length

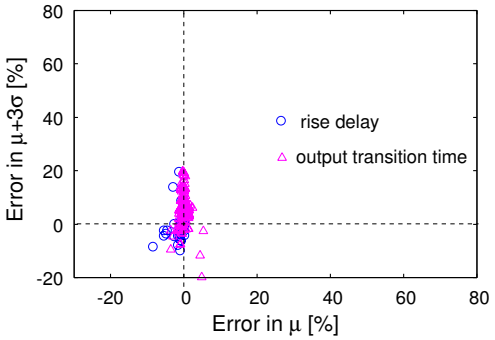

Fig. 12. Error in mean and worst between the proposed method and SPICE based Monte Carlo simulations under the variability of S_{AB}, input transition and gate length

V. Conclusions

In this paper, we discuss a statistical gate delay model for MIS. Most SSTA approaches assume a single input switching model and ignore the effect of MIS on gate delay. MIS occurs when multiple inputs of a gate switch nearly simultaneously. Thus, ignoring MIS causes the error in statistical maximum operation in SSTA. We propose a calculation method of gate delay and output transition time considering MIS. We compare the proposed method to Monte Carlo analysis of a transistor level simulation and show that the proposed method improves the error due to ignoring MIS. The proposed method can handle the variations of the input transition, the gate length and so on because the proposed method can be applied to the first-order canonical delay model.

The proposed method demands the gate delay as a function of S_{AB}. Therefore, the proposed method requires a large number of SPICE simulations for the cell library characterization process. Although this characterization is a one-time effort, our future works includes the reduction of cell characterization cost.

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