Super-K: A SoC for Single-chip Ultra Mobile Computer

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In this panel discussion, I will make a brief introduction to the on-going Super-K project at the Microprocessor Research and Development Center (MPRC). The background of this project is the convergence of computers, consumer electronics and communication, so called 3C. MPRC has a ten-year history in microprocessor and System-on-Chip (SoC) research and design. In the past, we have developed our own 32-bit RISC processor named UniCore, and two generations of SoC named PKUnity-863 (in acknowledgement of the support from China National High-Tech Program 863, abbr. 863 Project). From 2003 onwards, network computers based on UniCore have been used in commercial context.

In 2006, we launched the project called Super-K to design our next generation SoC, which will be the heart of a 3C computer also designed at MPRC. We named the project Super-K in the hope that the final product will be around 1000 RMB (one may remember another initiate, OLPC, targeted to a similar price zone).

If only one phrase is allowed to describe the distinct feature of Super-K, it would be this one: *a single-chip solution*. This is the only way to cut down cost to an extremely low level, and most likely, it is an effective way to achieve improved performance and power profile. Fortunately, MPRC is able to pursue this approach because we have our own processor and baseline SoC. The rest work is to integrate the other functionalities, such as memory controller, graphics, multimedia, network, and miscellaneous peripherals, on to the baseline SoC. This might be difficult for OLPC people and other system vendors, who merely purchase components and assembly them on board. It is unlikely for them to control the cost below $100 for a full-fledged computer.

The block diagram of the Super-K SoC is shown in Fig. 1. The boxes in blue color are the UniCore processor, and the boxes on the right-hand side are common peripherals that can be found in other PC chipsets. They are connected to the rest of the chip via a slow APB peripheral bus to the system high-speed AHB bus. Other IP modules for high-speed devices are on the bottom, most of which are purchased from IP vendors. They are connected to the AHB bus. To meet the bandwidth demand on bus and off-chip memory, two bus interfaces: one 32-bit and the other 64-bit one, are provided. The boxes on the left-hand side are multimedia accelerators and graphics components that are designed at MPRC.

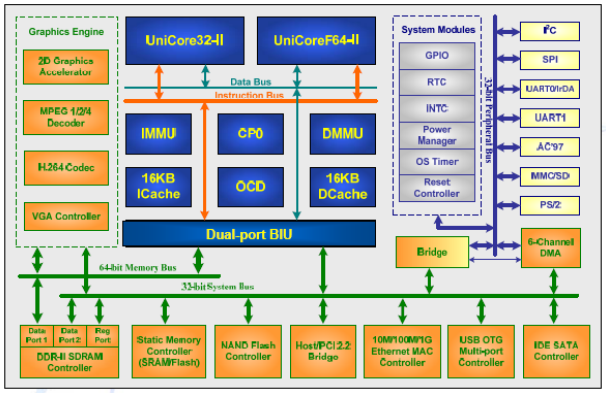

Fig. 1. Super-K SoC block diagram

In addition, there are at least three obvious benefits for this decision. First, it saves considerable cost by not purchasing an off-chip graphics card. Second, on-chip multimedia and graphics have a potential of higher performance due to the short latency of on-chip communication. Third, it can significantly reduce power consumption for similar reason.

Developing such a complex SoC is a non-trivial work. The project should be well planned and managed. A lot of challenges are expected to be encountered. Basically, the project is divided into the following sub-tasks, each one assigned to a corresponding team.

- UniCore: work on FP enhancement and DSP extension, as well as modifications to interfaces of the new SoC.
- UniGFX: work on the development of MPEG 1/2/4 multimedia accelerator, H.264 unit, a display engine, and a graphics engine
- SoC: work on the design, verification and integration of IP cores
- Modeling: work on transaction-level performance evaluation
- IC design: backend work, including floorplan, timing, power, signal integrity,...
- Software: work including porting Linux kernel 2.6, GNU toolchain, and popular applications onto UniCore architecture. Device driver development for various IPs is also an important part of the work.

Due to the space limitation, the challenges we encountered in the course of the Super-K project, as well as the experiences and lessons we learned will be shared with the audience during the panel discussion at ASP-DAC 2008.

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