Area and Power Efficient Design of Coarse Time Synchronizer and Frequency Offset Estimator for Fixed WiMAX Systems

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Abstract - Targeting fixed WiMAX systems, this paper presents a new architecture for coarse time synchronization and carrier frequency offset (CFO) estimation. The proposed architecture is based on a two-step approach where the data-paths are decoupled to individually optimize performance and area. Implemented with 0.13µm CMOS technology, the results show that the proposed architecture has advantages of less silicon area and power consumption as well as better performance compared to the previous joint approach.

I Introduction

The purpose of the coarse time synchronization is to detect the preamble. Since this synchronization has a significant effect on the overall performance and power consumption, it is one of the most important processing steps. The carrier frequency offset (CFO) estimation is also important, as it is critical to reduce the inter-channel interference. In the previous architectures, the CFO is jointly estimated with the coarse time synchronization based on the unified auto-correlator [2]. This approach is inefficient as the bit-width requirement of the coarse time synchronization is much smaller than that of the CFO estimation. For fixed WiMAX systems [1], this paper proposes a new decoupled architecture in which the coarse time synchronization and the CFO estimation are separately processed to reduce power and silicon area by performing individual optimization.

II. Proposed Architecture

The coarse time synchronization is performed by detecting the plateau of the auto-correlation of the received samples. In the previous architecture, a unified auto-correlator is used to jointly estimate the CFO along with the coarse time synchronization. This approach is inefficient in terms of power and area, as the coarse time synchronization requires much smaller bit-width than the CFO estimation does. The proposed architecture has two separate auto-correlators to optimize them individually, as shown in Fig. 1. It operates in two steps; a simple auto-correlator is employed for the coarse time synchronization, and then a precise auto-correlation is performed for the CFO estimation.

The normalized auto-correlation which corresponds to the upper part of Fig. 1 is used for the coarse time synchronization, where r_n is the n-th received sample quantized to a few bits. To derive a more efficient computation, the auto-correlation for the coarse time synchronization is implemented as a recursive structure as shown in Fig. 1. The sample buffer whose length is 128 is implemented as a circular buffer instead of a shift register to lower switching activity. As

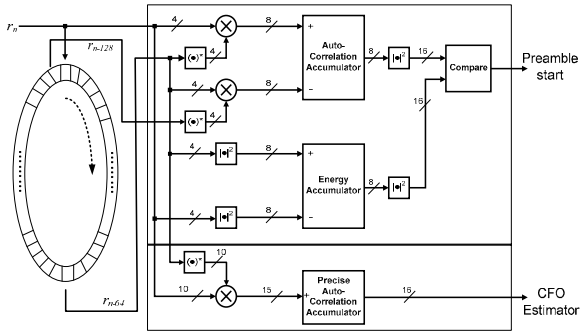

Fig. 1. Proposed architecture

shown in Fig. 2, the auto-correlation is efficiently implemented with four multipliers by extracting the common terms, while the straightforward structure needs eight multipliers. Additionally, the carry save addition is employed to add three operands in a more economical way.

A separate auto-correlator is used for the CFO estimation, as it needs a relatively high precision. In this case, the auto-correlation does not need to be normalized, since only the average phase difference is needed. Therefore, the multipliers and the accumulator needed for calculating energy can be eliminated as illustrated in Fig. 1. Moreover, the auto-correlation is calculated only once for one training sequence just after the coarse time synchronization is completed as shown in Fig. 3. It can be calculated with one complex multiplier and an accumulator more efficiently than the recursive form that needs two complex multipliers. The samples in the estimation window of the proposed architecture are guaranteed to be within the short training sequences, because they are taken after the coarse time synchronization is done. Therefore we can expect that the accuracy of the CFO estimation in the two step approach is significantly improved due to the purity of the samples involved, compared with the joint approach [2].

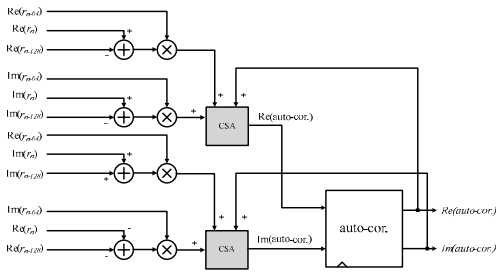

Fig. 2. Auto-correlator for the coarse time synchronization

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III. Evaluations

The performance is evaluated through simulations performed for SUI-3 multi-path fading channels [3]. The CFO in the channel is set to 1.7 sub-carrier spacings. The CFO estimation errors are compared in Fig. 4(a), where the proposed architecture performs auto-correlation for 128 samples coming after the coarse time synchronization and the joint approach shares the auto-correlation used for the coarse time synchronization [2]. As there is no ambiguity in selecting samples to be involved in the estimation, the proposed architecture shows better performance than the previous one. Fig. 4(b) compares the performance of the coarse time synchronization. We can see that the proposed architecture performs comparably to the previous architecture, even though the samples are represented in a much less bit-width.

Both the previous joint estimation and the proposed architecture are implemented with a 0.13μm CMOS standard cell library and synthesized under the same constraints. The gate counts are compared in Table I, counting a 2-input NAND cell as one. The proposed architecture achieves approximately 30% gate count reduction. As shown in Table II, the proposed architecture reduces the power consumption to about 40% compared to the previous one. As the synchronization in fixed WiMAX systems is as long as 2 MAC frames [1], this power reduction has a significant meaning. Fig. 5 shows a die-photo of the prototype chip designed based on the proposed architecture. Its size is about 500μm x 500μm.

IV. Conclusion

In this paper, we have proposed and implemented a new synchronization architecture for fixed WiMAX systems. In contrast to the previous joint approach, the coarse time synchronization and the CFO estimation are decoupled to optimize them individually in the proposed synchronization. The decoupled architecture is efficient not only in terms of power and area but also in performance. Compared to the previous joint approach, the proposed synchronization block reduces the silicon area and power consumption by 30% and 60%, respectively.

Acknowledgements

This work was supported by Korean Intellectual Property Office (KIPO) and IP design contest sponsored by Dongbu-Hitek.

References

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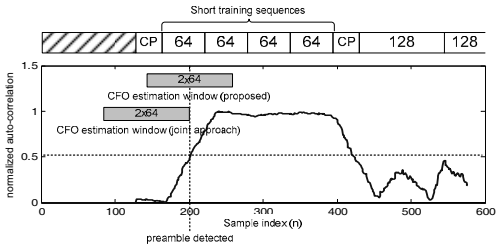
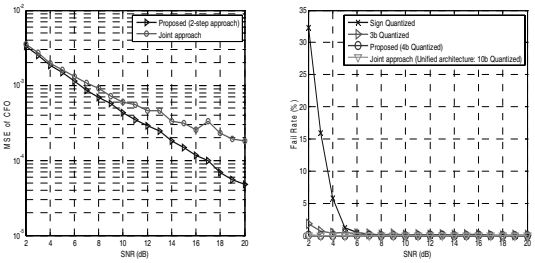


Fig. 3. CFO estimation window



(a) (b)

Fig. 4. Performance result (a) CFO estimation (b) Coarse time synchronization

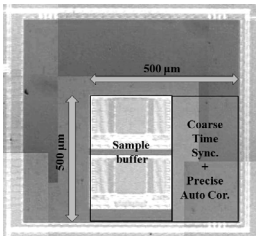


Fig. 5. Prototype chip

TABLE I
Power Consumption Comparison

SNR (dB)	Proposed (mW)	Joint Approach (mW)
2	6.195	14.630
8	6.123	16.331
14	5.876	15.680
20	5.769	15.917

TABLE II
Gate Count Comparison

	Proposed	Joint Approach
Precise auto-correlator	4232	11321
Coarse time synch.	3688	
Etc.	754	750
Total	8674	12071