A Wafer-Level Defect Screening Technique to Reduce Test and Packaging Costs for "Big-D/Small-A" Mixed-Signal SoCs*

Sudarshan Bahukudumbi† Sule Ozev† Krishnendu Chakrabarty† Vikram Iyengar‡

†Department of Electrical & Computer Engineering
Duke University, Durham, NC 27708
E-mail: {spb,sule,krish}@ee.duke.edu

‡IBM Microelectronics
Essex Junction, VT 05452
E-mail: vikrami@us.ibm.com

Abstract— Product cost is a key driver in the consumer electronics market, which is characterized by low profit margins and the use of a variety of "big-D/small-A" mixed-signal system-on-chip (SoC) designs. Packaging cost has recently emerged as a major contributor to the product cost for such SoCs. Wafer-level testing can be used to screen defective dies, thereby reducing packaging cost. We propose a new correlation-based signature analysis technique that is especially suitable for mixed-signal test at the wafer-level using low-cost digital testers. The proposed method overcomes the limitations of measurement inaccuracies at the wafer-level. A generic cost model is developed to evaluate the effectiveness of wafer-level testing of analog and digital cores in a mixed-signal SoC, and to study its impact on test escapes, yield loss and packaging costs. Experimental results are presented for a typical mixed-signal "big-D/small-A" SoC, which contains a large section of flattened digital logic and several large mixed-signal cores.

I. Introduction

Rapid advances in the semiconductor industry and in design tools have led to the integration of digital and analog cores in mixed-signal system-on-chip (SoC) integrated circuits. The fraction of die area taken up by analog circuits can range from 5% to 30% for a typical mixed-signal SoC [1]. The DragonBall^{TM}-MX1 SoC, details for which are presented in [2], is an example of a "big-D/small-A" mixed-signal SoC. The applications of mixed-signal SoCs to the consumer market are numerous, ranging from medical monitoring devices to audio products and handheld devices. The consumer electronics market is also characterized by low profit margins and rising packaging costs [3, 4]. Test and packaging costs are therefore of increasing importance for such SoCs.

The test cost for a mixed-signal SoC is significantly higher than that for a digital SoC [5]. This is due to the capital cost associated with expensive mixed-signal automatic test equipment (ATE), as well as the high test times for analog cores. Test methods for analog circuits that rely on low-cost digital testers are therefore especially desirable; a number of such methods have recently been developed [6, 7].

It is well-known that wafer-level testing leads to early defect screening, thereby reducing packaging and production cost [8, 9]. As highlighted in [3, 4], packaging cost accounts for a significant part of the overall production cost. Current packaging costs for a cost-sensitive, yet performance-driven IC can vary between \$3.60 to \$20.50, depending on the number of pins in the IC [3]. It has also been reported that the packaging cost per pin exceeds the cost of silicon per square millimeter, and the number of pins per die can easily exceed the number of square millimeters per die [3, 4]. These trends highlight the need to minimize the cost associated with the packaging of faulty dies by effective testing at the wafer-level. The impact of packaging cost on the overall production cost provides a major motivation for the work presented in this paper.

Despite the numerous benefits of testing at the wafer level, industry practitioners have reported that mixed-signal test is seldom carried out at the wafer level [10]. Measurement inaccuracies are common when analog cores are tested in a mixed-signal test environment based on digital signal processing. This problem is exacerbated by noisy DC power supply lines, improper grounding of the wafer probe, and lack of proper noise shielding of the wafer probe station [11]. The above problems make test and characterization at the wafer-level especially difficult, and they can lead to high yield loss during wafer sort. Moreover, since test time is a major practical constraint for wafer sort, even more so than for package test, not all scan-based tests can be applied to the digital cores under test [12].

In this paper, we present a new correlation-based signature analysis technique for mixed-signal cores, which facilitates defect screening at the wafer-level. The proposed technique is inspired by popular outlier analysis techniques for IDDQ testing [13, 14]. Outlier identification using IDDQ during wafer sort is difficult for deep-submicron processes [14]. This problem has been addressed using statistical post-processing techniques that utilize the test response data from the ATE [13]. We propose a similar classification technique that allows us to make a pass/fail decision under non-ideal ambient conditions and using imprecise measurements. We present a wafer-scale analog test method based on the use of low-cost digital testers, and with reduced dependence on mixed-signal testers.

A comprehensive cost model is needed to evaluate the effectiveness of wafer-level testing, and its impact on test and packaging cost. We develop a cost model and use it to quantify the benefits derived from wafer-level testing of both analog and digital cores. Correction factors, which account for the misclassification of dies under test, are incorporated in the cost model. Experimental results involving the wafer-level test technique as well as the cost model are presented for an industrial mixed-signal SoC. The results show that a significant re-

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duction in product cost can be obtained using wafer-level testing and the proposed signature analysis method.

The remainder of the paper is organized as follows. Section II describes the proposed signature analysis method for wafer-level test of analog cores. Simulation results are presented to evaluate the signature analysis method. Section III describes the cost model for a generic mixed-signal SoC. Section IV details the reduction in product cost that can be obtained using wafer-level testing for an industrial mixed-signal SoC. Finally, Section V presents conclusions and outlines directions for future work.

II. Wafer-Level Defect Screening: Mixed-Signal Cores

Test procedures for data converters can be classified as being based on either spectral-based tests or code density tests. Spectral-based test methods [15] usually involve the use of a suitable transform, such as the Fourier Transform, to analyze the output. These methods are used to determine the dynamic test parameters of the data converter. On the other hand, code density tests are based on the constructions of histograms of the individual code counts [16]. The code counts of the data converter-under-test are then analyzed and compared with the expected code counts to determine its static parameters. Recent work in mixed-signal testing has focused on spectral-based frequency domain tests, due to the inherent advantage of test time over the code density tests. In [15], a test flow process is described, that uses only the dynamic tests. A case study on sample data converters presented in [15] claims that 96% of faults involving both static and dynamic specifications can be detected without using the code density test technique. It is important to note that the procedure described in [15] is aimed at production testing. In [17], it has been shown that frequency-domain-based signature analysis helps in suppressing non-idealities associated with the test data, and it serves as a robust mechanism for enhancing fault coverage and reducing false alarms.

In effect, a mixed-signal path can be sandwiched between a pair of complementary data converters to generate a mixed-signal core driven by digital inputs and outputs [7]. Testing this mixed-signal path, which is a basic building block in most "big-D/small-A" SoC designs, holds key to cost effective testing using low cost digital testers. The inadequacy of analog tests and their lack of effectiveness at wafer sort to accurately measure test parameters and identify faulty dies have been highlighted in [10] and [18].

Measurement inaccuracies associated with a mixed-signal test and measurement environment are described in [7, 11]. These problems can lead to a degradation in the quality of the measurements made; these effects are more pronounced at wafer sort [11]. As a result, yield loss and test escape are more likely at the wafer-level.

Test procedures examine the output response of the circuit and compare it to a pre-determined "acceptable" signature. In light of all the possible error sources during wafer sort, a reliable acceptable signature is hard to derive because it requires the modeling of all possible errors. To address the above problems, outlier analysis has been extensively used in the IDDQ testing of digital circuits [13]. We employ a similar pass/fail criterion in the proposed wafer-level testing approach. To perform such an analysis, we first require a measurable parameter for each core. In IDDQ testing, this data comes in the form of supply current information. However, in spectral analysis, the information obtained as a signature is spread over multiple data points, where each data point represents the power associated with the corresponding frequency bin. It is therefore necessary to encode this information as a single parameter corresponding to each individual core. We propose two correlation-based test methods to achieve this goal. These methods are referred to as the *mean-signature*- and *golden-signature*-based correlation techniques.

A. Signature Analysis: Mean-Signature-Based-Correlation (MSBC)

In [17], the authors use the correlation between a reference spectrum and the spectrum of the circuit under test as a pass/fail criterion. The reference spectrum serves as an acceptable signature, and is used for comparison with the spectrum of the circuit under test. Such a reference signature is called an Eigen signature [17]. The sensitivities to changes in the shape of the spectrum of the device-under-test from the Eigen signature can be quantified by means of a correlation parameter. The correlation is a fraction that lies between 0 and 1, and it serves as a single measurable parameter for each individual die.

The characteristic spectrum X_i of the i^{th} core-under-test in a batch of m identical cores is obtained using a P-point Fast Fourier Transform (FFT) and is defined as: $X_i = \{x_{i1}, x_{i2}, ...x_{iP}\}$, $1 \leq i \leq m$. The elements $x_{i1}, x_{i2}, ...x_{iP}$ in the above spectrum denote the power associated with the corresponding frequency bin. Ideally, the spectrum of each die should be correlated to a set of averages of the spectra of m dies tested under similar ambient operating conditions. The Eigen signature E is determined as the set of averages of the spectra of m identical cores-under-test and can be defined as: $E = \{(\sum_{i=1}^{m} x_{i1})/m, (\sum_{i=1}^{m} x_{i2})/m, \cdots, (\sum_{i=1}^{m} x_{iP})/m\}$. In particular, if the number of good dies is appreciably larger than the number of defective ones, the Eigen signature contains the information needed to classify the good dies from the defective ones. Since both X_i and E are random variables, let $\overline{X}_i$ and $\overline{E}$ represent the mean of X_i and E respectively. The correlation between the Eigen spectrum and that of the circuit under test can now be defined using Equation (1) as:

$$\mathrm{corr}(X_i, E) = \frac{\sum_{j=1}^{P}(x_{ij} - \overline{X}_i)\left(\frac{\sum_{i=1}^{m} x_{ij}}{m} - \overline{E}\right)}{\left[\sum_{j=1}^{P}(x_{ij} - \overline{X}_i)^2 \sum_{j=1}^{P}\left(\frac{\sum_{i=1}^{m} x_{ij}}{m} - \overline{E}\right)^2\right]^{1/2}} \quad (1)$$

B. Signature Analysis: Golden-Signature Based-Correlation (GSBC)

For the MSBC technique, the collection of spectral signatures requires the storage of spectral information of a number of dies before a pass/fail decision can be made. While this information does not have to reside in the main memory of the

tester, storing and handling such a large amount of data may be inconvenient. It may be desirable to use a pre-defined *golden-signature* for correlation during wafer sort. It is important to note that the use of a pre-defined spectrum as the *golden signature* does not hamper outlier analysis. The *golden-signature* spectrum is obtained *a priori*, by assuming ideal and fault-free operating conditions for the circuit under test. The correlation parameter can still be used to identify the possible faulty dies. The correlation parameters are estimated in the same way as in Section II.A. The only difference here lies in the use of a *golden signature* as the Eigen signature. The test flow for both methods is described in Fig. 1.

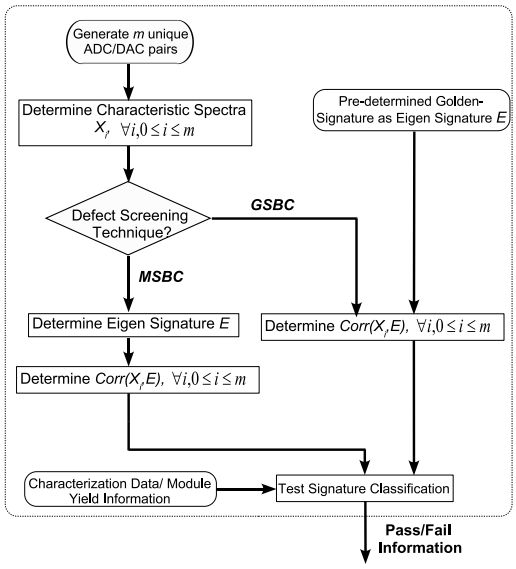

Fig. 1. Flowchart depicting the mixed-signal test process for wafer-level fault detection.

The next step in signature analysis is to set a threshold to determine the pass/fail criterion for each die. As explained previously, due to all the non-idealities in the measurements, a pre-determined threshold is of little use. However, during wafer sort, characterization data on mixed-signal components is already available. The characterization data provides information on the approximate percentage of dies that are expected to pass the final test. Modular testing of SoCs can also provide information on the approximate yield per module/core in an SoC [19]. Characterization information, in conjunction with the module yield data, can be used to estimate *a priori*, the approximate number of dies that will pass the test. The yield loss due to this indirect testing method should be minimized, since yield loss affects overall cost by increasing the effective cost of silicon per unit die. The number of passing dies can be estimated by using the expected yield ($Y_{\%}$) information from the characterization data. We set the fraction of the number of dies passing the test to be $Y_{\%} + \frac{(100-Y_{\%})}{k}$. The constant k can be chosen based on the type of signature analysis technique used.

C. Experimental Results

The effectiveness of the proposed methods can be established by determining the resultant yield loss and test escapes. If G represents the number of good circuits and G_{fail} the number of good circuits failing the test, then the yield loss can be estimated to be $\frac{G_{fail}}{G}$. The number of faulty circuits that pass the test (F_{pass}) can be used to calculate the test escapes as $\frac{F_{pass}}{N-G}$.

Correlation Technique	FFT No. of Sample Points-Yield Type	YL (%)	OTE (%)	TE_{MaF}(%)	TE_{MoF}(%)	TE_{GF}(%)
Mean Signature	1024-LY	0.8176	46.66	89.25	33.21	3.53
	1024-MY	0.25	67.7	97.11	66.19	0
	1024-HY	0.9	49	95.23	54	7.4
	4096-LY	0.06	47	77.1	7.95	0
	4096-MY	0.08	27.43	58.65	12.67	0
	4096-HY	0	25	95.23	10	0
Golden Signature	1024-LY	1.006	75.71	98.59	73.7	42.47
	1024-MY	0.0375	68.75	96.15	67.6	5
	1024-HY	1.1	74	100	76	55.55
	4096-LY	0.18	29.78	88.31	7.95	0.88
	4096-MY	0.16	43.36	96.15	15.49	0
	4096-HY	0.1	2.5	100	8	0

TABLE I
WAFER-LEVEL DEFECT SCREENING: EXPERIMENTAL RESULTS FOR AN 8-BIT FLASH ADC.

To evaluate the above performance metrics, we develop a behavioral model of a flash-type ADC in MATLAB. We generate 1500 unique circuit instances of the ADC by inducing parametric variations in the associated components and also by injecting certain hard and soft failure types. The hard failure type corresponds to catastrophic failures and the soft failure type corresponds to parametric variations that result in undesirable circuit operation. The hard faults are generated for 100 data converters by forcing resistive opens and broken lines in the comparator network. We then vary the component parameters; the values of resistors and the offset voltages of the comparators, to generate three sets of data converters. We modify the standard deviations of resistor values and offset voltages to randomly inject the soft faults. The three sets of data converters correspond to high yield (HY-90%), moderate yield (MY-75%) and low yield (LY-60%). Correlation parameters for each unique ADC are obtained for both the proposed methods and by using a 1024-point and a 4096-point FFT. In this experiment, the specification that determines the good/faulty dies is the differential-non-linearity (DNL) parameter. The acceptable range of DNL for the ADC is set to be $0 \le DNL \le 0.5$. Based on the random fault injection scheme, we have a number of marginally faulty dies ($0.5 \le DNL \le 1$), moderately faulty dies ($1 \le DNL \le 2$) and grossly faulty dies ($DNL > 2$). The percentages of marginal, moderate and grossly faulty data converters in the overall population are 44%, 37% and 19% respectively.

We present experimental results for the 8-bit flash ADC model in Table I. It is clear that the MSBC technique outperforms the GSBC technique in most cases, both in terms yield loss (YL) and overall test escapes (OTE). Table I lists the percentage of test escapes for marginal (TE_{MaF}), moderate (TE_{MoF}), and grossly (TE_{GF}) faulty dies. The percentages are given in terms of the number of faulty dies in each group). Columns 5-7 list the relevant data separately for each fail type. As a result, the rows of the table for these three columns do not add up to 100%. This analysis is performed in order to evaluate the effectiveness of our proposed signature analysis techniques over different failure regions. A significant percentage of marginal failures result in test escapes. This shows that the proposed signature analysis technique is not effective for screening marginal failures. On the other hand, 33%–92% and 26%–92% of the moderately faulty dies are screened in the case of the MSBC technique and GSBC technique, respectively. Thus our technique is effective for screening moderate

and gross failures, which is typically the objective in wafer-level testing. Marginal failures are best detected at package test, where the chip can be tested in a more comprehensive manner.

III. Generic Cost Model

In this section, we present a cost model to evaluate wafer-level testing for a generic mixed-signal SoC. A cost model for an entire electronic assembly process is described in [20], using the concept of "yielded cost". However, it cannot be readily adapted for wafer-level testing. In [9], a cost modeling framework for analog circuits was proposed, but it did not explicitly model the precise relationship between yield loss, test escape and the overall product cost. The effects of yield loss and test escape for both the digital and mixed-signal cores in an SoC is modeled in our unified analytical framework. The proposed model also considers the cost of silicon corresponding to the die area.

A. Correction Factors : Test Escapes and Yield Loss

Testing at the wafer level leads to yield loss and test escapes. Yield loss occurs when testing results in the misclassification of good dies as being defective, and the dies are not sent for packaging. We use the term Wafer-Test-Yield Loss (WYL), to refer to the yield loss resulting from wafer-level testing, and the associated non-idealities. Clearly, WYL must be minimized to reduce product cost.

The test escape component is also undesirable, due in large part to the mandated levels of shipped-product quality-level (SPQL), also known as defects per million, which is a major driver in the semiconductor industry. SPQL is defined as the fraction of faulty chips in a batch that is shipped to the customer. Test escapes at the wafer-level are undesirable because they add to packaging cost, but they do not increase SPQL if these defects are detected during module tests.

In order to make the cost model robust, we introduce correction factors to account for the test escapes and WYL. The correction factor for test escapes is obtained from the "fault coverage curve", which shows the variation of the fault coverage versus the number of test vectors. It has been shown in [8], and more recently in [21], that, the fault coverage curve can be mapped to a log function of the type $fc_n = 1 - \alpha e^{-\beta n}$, where n is the number of test patterns applied, fc_n is the fault coverage for n test patterns, α and β are constants specific to the circuit under test and the fault model used.

Typically in wafer-level testing for digital cores, only a subset of patterns are applied to the circuit, i.e., if the complete test suite contains n patterns, only $n^* \leq n$ patterns are actually applied to the core-under-test. The correction factor θ_{n^*}, defined as $\theta_{n^*} = \frac{(fc_n - fc_{n^*})}{fc_n}$, $0 \leq n^* \leq n$, is used in the model to account for test escapes during wafer-level testing.

Fig. 2 shows how the fault coverage varies as a function of the number of applied test vectors for the digital portion of a large industrial ASIC, which we call Chip K [22]. The digital logic in this chip contains 2,821,647 blocks (including approximately 334,000 flip-flops), where a block represents a cell in the library. The figure also shows the correction factor as a function of the number of test vectors applied to the same circuit. Section II showed how we can evaluate the test escapes for analog cores. Let us assume that the test escape for analog cores is β. Assuming that test escapes for the analog cores are independent from the test escapes for digital cores (a reasonable assumption due to the different types of tests applied for the two cores), the SoC test escape can be estimated to be $1 - (1 - \theta_{n^*}) \cdot (1 - \beta)$. Let us now consider the correction

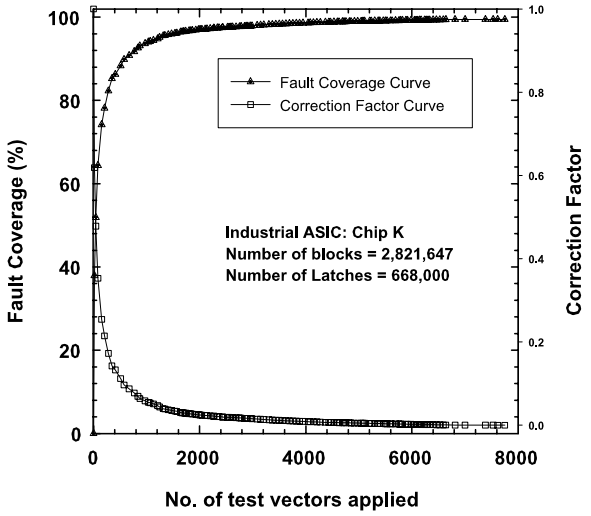

Fig. 2. The variation of the fault coverage and correction factor versus the number of test vectors applied to the digital portion of Chip K [22].

factor due to WYL. If the WYL for the digital part of the SoC is WYL_d and that for the analog part of the SoC is WYL_a, the effective WYL for the SoC is simply given by $WYL_{eff} = 1 - (1 - WYL_d) \cdot (1 - WYL_a)$. The parameter WYL_d can be negligible if overtesting, which is a major concern nowadays for production testing of digital circuits [23], is not significant at the wafer-level. However, the parameter WYL_a cannot be neglected for the reasons described in Sections I and II.

B. Cost Model: Generic Framework

We now present our generic cost model. The cost model treats the outcomes of a test as random variables and assigns probabilities to the different possible outcomes. Appropriate conditional probabilities are used to ensure that the model takes all possible scenarios into account. Let us first define the following events: T^+: the event that the test passes, i.e., the circuit is deemed to be fault-free; T^-: the event of the test fails, i.e., the circuit is deemed to be faulty; D^+: the event that the die is fault-free; D^-: the event that the die is faulty.

Conditional probabilities associated with the above events help us to determine the various factors that influence overall test, packaging and silicon cost. The following conditional probabilities are of interest—$P(T^+ \mid D^-)$: Probability of a test pass for a faulty die (representative of test escapes); $P(T^+ \mid D^+)$: Probability of a test pass for a good die (correct classification of a good die); $P(T^- \mid D^-)$: Probability of a test fail for a bad die (correct defect screening); $P(T^- \mid D^+)$: Probability of a test fail for a good die (representative of WYL).

Using the above conditional probabilities, we can derive the following expressions for $P(T^+)$ and $P(T^-)$:

$$P(T^+) = P(T^+ \mid D^+)P(D^+) + P(T^+ \mid D^-)P(D^-) \quad (2)$$

$$P(T^-) = P(T^- \mid D^+)P(D^+) + P(T^- \mid D^-)P(D^-) \quad (3)$$

where, $P(T^+) = 1 - P(T^-)$.

$P(T^+ \mid D^-)$ denotes the test escape, while $P(T^- \mid D^+)$ indicates the yield loss. Note that $P(D^+)$ represents the yield Y of the process and $P(D^-) = 1 - P(D^+)$. Knowing these parameters, we can calculate $P(T^-)$ using Equation (3). Solving for $P(T^+ \mid D^+)$ from the above equations, we get:

$$P(T^+ \mid D^+) = (1 - P(T^-) - (P(T^+ \mid D^-)P(D^-))/P(D^+) \quad (4)$$

The probability $P(T^+)$ represents the fraction of the total number of dies that need to be packaged. The conditional probability $P(T^+ \mid D^+)$ represents the number of good dies that are packaged i.e., it represents the fraction of dies for which the test passes when the die is fault-free. This conditional probability, which can be easily calculated using Equation (4), is used to calculate the effective cost per unit die from the overall test and manufacturing costs.

C. Overall Cost Components

The overall production cost depends on whether only after-package testing is carried out, or if wafer-level testing is done in addition to production testing. We first determine the cost when only after-package testing is carried out. Let the total number of dies being produced be N, let t_{ap} represent the total test application time at the production level and c_{ap} represent the cost of test application (in \$) per unit time during after-package testing. Let C_P denote the cost of packaging per unit die, A_{die} be the area of the die under consideration, and C_{sil} be the cost of silicon (in \$) per unit area of the die. The overall production cost $C_{oc_{ap}}$ (that includes test time cost and silicon area cost, but ignores other cost components not affected by the decision to do wafer-level testing) associated with manufacturing a batch of N dies can now be determined using Equation (5):

$$C_{oc_{ap}} = (N \cdot t_{ap} \cdot c_{ap}) + N \cdot C_P + (N \cdot A_{die} \cdot C_{sil}) \quad (5)$$

Similarly the overall cost ($C_{oc_{wap}}$) associated with the manufacture of a batch of N dies for which both wafer-level and after-package testing are performed can be determined using Equation (6).

$$C_{oc_{wap}} = (N \cdot t_w \cdot c_w) + P(T^+) \cdot N \cdot C_P + (P(T^+) \cdot N \cdot t_{ap} \cdot c_{ap}) + (N \cdot A_{die} \cdot C_{sil}) \quad (6)$$

In Equation (6), t_w and c_w represent the overall test time at the wafer-level and the tester cost per unit time, respectively. Recall that $P(T^+)$ represents the fraction of dies that pass the test at the wafer-level. This is an indicator of the number of dies to be packaged and tested at the production level. The cost per unit die by performing wafer and production level tests ($C_{die_{wap}}$) can be calculated from Equations (5) and (6) as $C_{oc_{wap}}/(N \cdot Y \cdot P(T^+ \mid D^+))$. When only production level tests are performed the cost per unit die can be estimated to be $C_{oc_{ap}}/(N \cdot Y)$. This estimate of the cost per unit die is overly optimistic because we assume that there is no yield loss or test escape associated with after-package testing. This is usually not the case in practice. We can now define the cost savings as $(\delta C = C_{oc_{ap}}/(N \cdot Y)) - (C_{oc_{wap}}/N \cdot Y \cdot P(T^+ \mid D^+))$, which indicates the reduction in production cost per die due to the use of wafer-level testing.

IV. Cost Model: Quantitative Analysis

In this section, we use the model to validate the importance of wafer-testing from a cost perspective. In order to use the cost model, we need realistic values of the cost components used in the model. For this purpose, we model the section of flattened digital logic (as explained in Section III) as a single core, and use relevant information from a commercial mixed-signal SoC, Chip U [22]. The mixed-signal SoC includes a pair of complementary data converters of identical bit-resolution. The data converters can be configured in such a way that each DAC is routed through the ADC for purposes of test (as explained in Section II). It is appropriate to assume that the ADC and the DACs are tested as pairs because a single point of failure is a sufficient criterion to reject the IC as being faulty.

In [4], the importance of packaging is highlighted with realistic numbers on the cost of silicon and cost of packaging per unit die. Furthermore, [1, 24] provides actual packaging costs for various types of packages. In this section, we choose the cost of packaging per die after carefully studying the published data. The package cost is varied from \$1 per die to \$9 per die, which is considerably lower than published data. Lower values of package costs are considered for smaller dies. Since the cost model for wafer-level testing will predict more cost savings for higher package costs, we choose lower values for the package cost to ensure that there is no bias in the results. Packaging costs for a high-end IC can be as high as \$100 per die [4, 24, 3]. The cost of silicon from [4] is estimated to be \$0.1 per unit mm^2. We consider three typical die sizes from industry (10mm^2, 40mm^2 and 120mm^2) corresponding to small, medium and large dies, for purposes of simulation. We use a typical industry "yield curve" [22], shown in Fig. 3, to illustrate the spread in cost savings than is achieved by testing mixed-signal SoCs at the wafer level. The points on the yield curve correspond to the probability that the yield matches the corresponding point on the x-axis. The yield curve is appropriately adjusted to reflect distributions corresponding to die sizes; higher yield numbers are optimistic for large dies, and vice versa [25].

A. Cost Model: Results for ASIC Chip K

Test costs typically range from \$0.07 per second for an analog tester to \$0.03 per second for a digital tester [22]. The cost is further reduced dramatically for an old tester, which has depreciated from long use to a fraction of a cent per second. The proposed wafer-level test method benefits from lower test time costs, hence to eliminate any favorable bias in our cost evaluation, we assume that the test time cost is an order of magnitude higher, i.e., \$0.30 per second.

We model the test escapes by assuming that the the digital portion ASIC Chip K [22] is tested with 4046 test patterns, and for which the test escape correction factor is calculated from Fig. 2. The analog test time is modeled by assuming that the data converter pair is tested with a 4096-point FFT. The test escape of the mixed-signal portion of the chip is assumed to be 50%.

Figures 3–4 illustrate the effect of varying packaging costs on δC for small and large dies, respectively. The cost savings per die are analyzed for each point in the discretized yield

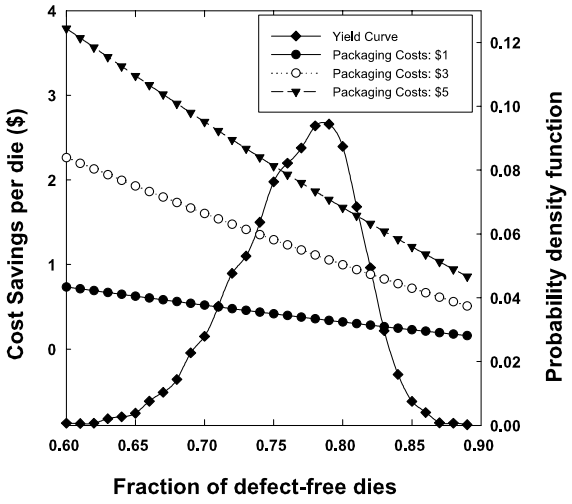

Fig. 3. Distribution of cost savings for a small die with packaging costs of (a) $1 (b) $3 (c) $5.

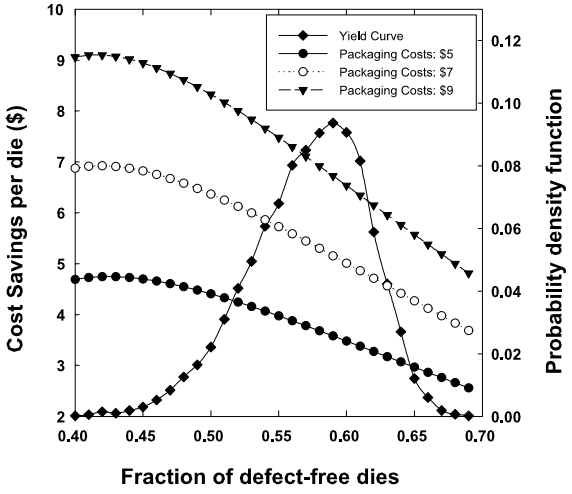

Fig. 4. Distribution of cost savings for a large die with packaging costs of (a) $5 (b) $7 (c) $9.

curve. This is done in order to illustrate the spread in cost saving that can be achieved in a realistic production environment. It is evident that the savings that can be achieved by performing wafer level tests is significant, and that it decreases with increase in yield.

V. Conclusions

We have proposed a wafer-level defect screening technique for core-based mixed-signal SoCs. Two new correlation-based signature analysis methods have been presented for wafer-level testing of analog cores. A comprehensive cost model has been developed for a generic mixed-signal SoC; this model allows us to quantify the savings that result from wafer-level testing. Test escape, yield loss, and packaging have been incorporated in this production cost model. We have used an industrial mixed-signal SoC to evaluate the proposed wafer-level test method. The proposed method uses a low-cost digital tester for wafer-level mixed-signal test, which further reduces test cost.

References

[1] R Brederlow et al., "A mixed-signal design roadmap," *IEEE Design & Test*, vol. 18, pp. 34–46, Nov. 2001.

[2] G. Bao, "Challenges in low cost test approach for ARM^{tm} core based mixed-signal SoC DragonBall^{tm}-MX1," in *Proc. ITC*, 2003, pp. 512–519.

[3] International Technology Roadmap for Semiconductors: Assembly and Packaging, *http://www.itrs.net/Links/2005ITRS/AP2005.pdf,* 2005.

[4] A. B. Kahng, "The road ahead: The significance of packaging," *IEEE Design & Test*, vol. 19, pp. 104–105, Nov. 2002.

[5] B. Koupal and T. Lee and B. Gravens. Bluetooth Single Chip Radios: Holy Grail or White Elephant, *http://www.signiatech.com/pdf/paper two chip.pdf*.

[6] C. Pan and K. Cheng, "Pseudo-random testing and signature analysis for mixed-signal circuits," in *Proc. ICCAD*, 1995, pp. 102–107.

[7] C. Taillefer and G. Roberts, "Reducing measurement uncertainty in a DSP-based mixed-signal test environment without increasing test time," *IEEE Trans. VLSI Systems*, vol. 13, pp. 862–861, Jul. 2005.

[8] M. Bushnell and V. Agrawal, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits*. Kluwer, 2000.

[9] S. Bhattacharya and A. Chatterjee, "Optimized wafer-probe and assembled package test design for analog circuits," *ACM Trans. Design Automation of Electronic Systems*, vol. 10, pp. 303–329, Apr. 2005.

[10] J. Sweeney and A. Tsefrekas, "Reducing test cost through the use of digital testers for analog tests," in *Proc. ITC*, 2005, pp. 1–9.

[11] W. Lau, "Measurement challenges for on-wafer RF-SOC test," in *Proc. Electronics Manufacturing Tech. Symp.*, 2002, pp. 353–359.

[12] P. C. Maxwell, "Wafer-package test mix for optimal defect detection and test time savings," *IEEE Design & Test of Computers*, vol. 20, pp. 84–89, Sep. 2003.

[13] W. R. Daasch et al., "Neighbor selection for variance reduction in IDDQ and other parametric data," in *Proc. ITC*, 2001, pp. 1240–1249.

[14] A Keshavarzi et al., "Multiple-parameter CMOS IC testing with increased sensitivity for IDDQ," *IEEE Trans. VLSI Sys.*, vol. 11, pp. 863–870, Oct. 2003.

[15] S. Bernard et al., "A new methodology for ADC test flow optimization," in *Proc. ITC*, 2003, pp. 201–209.

[16] A. Frisch and T. Almy, "HABIST: histogram based analog built in self test," in *Proc. ITC*, 1997, pp. 760–767.

[17] E. Acar and S. Ozev, "Delayed-RF based test development for FM transceivers using signature analysis," in *Proc. ITC*, 2004, pp. 783–792.

[18] M. d'Abreu, "Noise – its sources, and impact on design and test of mixed signal circuits," in *Proc. Workshop on Electronic Design, Test and Applications*, 1997, pp. 370–374.

[19] U. Ingelsson et al., "Test scheduling for modular SOCs in an abort-on-fail environment," in *Proc. ETS*, 2005, pp. 8–13.

[20] D. E. Becker and A. Sandborn, "On the use of yielded cost in modeling electronic assembly processes," *IEEE Trans. Electronics Packaging Manufacturing*, vol. 24, pp. 195–202, Jul. 2001.

[21] S. Edbom and E. Larsson, "An integrated technique for test vector selection and test scheduling under test time constraint," in *Proc. ATS*, 2004, pp. 254–257.

[22] ASICs Test Methodology, IBM Microelectronics, Essex Jct, VT 05452.

[23] G. Chen et al, "Procedures for identifying untestable and redundant transition faults in synchronous sequential circuits," in *Proc. ICCD*, 2003, pp. 36–41.

[24] http://www.mosis.org.

[25] M. Shen et al., "Cost and performance analysis for mixed-signal system implementation: System-on-chip or system-on-package," *IEEE Trans. Electronics Packaging Manufacturing*, vol. 25, pp. 522–545, Oct. 2002.