ASP-DAC 2006 Technical Program Committee

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[1] System Level Design Methodology

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[2] Embedded and Real-Time Systems

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[3] Behavioral/Logic Synthesis and Optimization

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[4] Validation and Verification for Behavioral/Logic Design

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[5] Physical Design (Routing)

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[6] Physical Design (Placement)

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[7] Timing, Power, Signal/Power Integrity Analysis and Optimization

∗**Sachin Sapatnekar**
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Jin-Jia Liou
National Taiwan University
Takashi Sato
Renesas
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University of California, Riverside
Ryuichi Yamaguchi
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[8] Interconnect, Device and Circuit Modeling and Simulation

∗**Hideki Asai**
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Charlie Chung-Ping Chen
National Taiwan University
Eli Chiprout
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Hiroo Masuda
STARC
Jae-Kyung Wee
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[9] Test and Design for Testability

∗**Seiji Kajihara**
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Sungho Kang
Yonsei University
XiaoWei Li
China Academy of Sciences
Prab Varma
Veritable

[10] Analog, RF and Mixed Signal Design and CAD

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Seijiro Moriyama
PDF Solutions
Hong-June Park
POSTECH
Jaijeet Roychowdhury
University of Minnesota
Chau-Chin Su
National Chao-Tung University

[11] Leading Edge Design Methodology for SOCs and SIPs

∗**Hideharu Amano**
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Satoshi Matsushita
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In-Cheol Park
KAIST
Ing-Jer Huang
National Sun-Yat-Sen University
Borivoje Nikolic
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