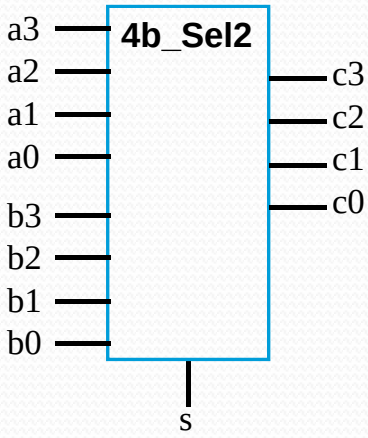
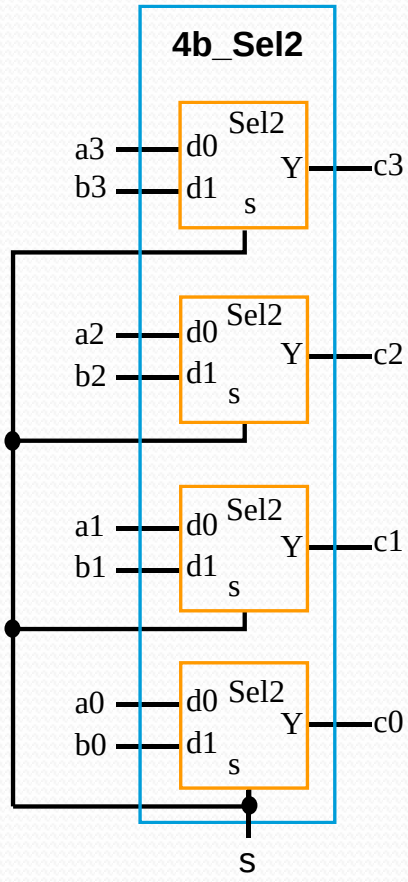
Hierarchical Composition






```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY 4b_Sel2 IS
   PORT (a3, a2, a1, a0: IN std_logic;
         b3, b2, b1, b0: IN std_logic;
         s: IN std logic;
         c3, c2, c1, c0: OUT std_logic);
END 4b_Sel2;

ARCHITECTURE 4b_Sel2_str OF 4b_Sel2 IS
   COMPONENT Sel2 IS
      PORT (d1, d0, s: IN std_logic;
            Y: OUT std_logic);
   END COMPONENT;

BEGIN
   Sel2_3:  Sel2  PORT MAP (b3, a3, s, c3);
   Sel2_2:  Sel2  PORT MAP (b2, a2, s, c2);
   Sel2_1:  Sel2  PORT MAP (b1, a1, s, c1);
   Sel2_0:  Sel2  PORT MAP (b0, a0, s, c0);
END 4b_Sel2_str;
```