Lab 1: XOR Gate Example

Digital Design Lab

Overview

- Lab 1 methodology
- XOR gate example
  - Lab procedure walkthrough

Methodology

Before creating the VHDL code, we should do the following:

1. Understand the problem

2. Derive the truth table
3. Derive a minimal Boolean expression
4. Optimize Boolean expression for the given gate library
5. Estimate input/output delay

6. Write behavioral model with estimated time (see VHDL videos)
7. Simulate and submit the behavioral model

8. Write the structural model (see VHDL videos)
9. Simulate the structural model and compare simulation results
10. Submit the structural model

XOR Example: Problem Description

Problem:

Represent an XOR gate using only NOR gates (1.4 ns delay each).

1. Understand the Problem

What is an XOR gate?

- How can an XOR gate be represented?

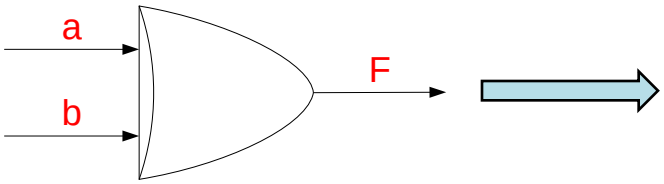
What is a NOR gate?

- Can NOR gates represent an XOR gate?

What steps do we need to perform to get to the NOR representation of XOR?

2-4. Truth Table and Expressions

XOR Gate



Inputs		Output
a	b	F
0	0	0
0	1	1
1	0	1
1	1	0

a \ b	0	1
0	0	1
1	1	0

Now represent as NOR gates through
a series of transformations using Boolean Algebra

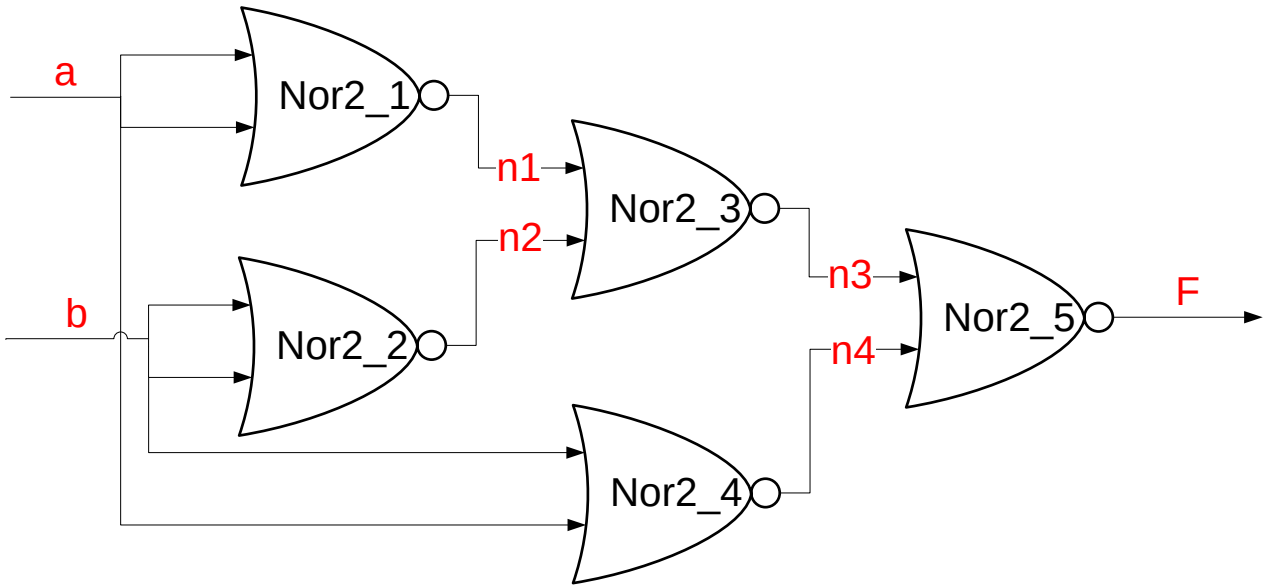
F = a'b + ab' -- from K-Map
F = (a + b')' + (a' + b)' -- De Morgan's Theorem
F = ((a + b')(a' + b))' -- De Morgan's Theorem
F = (aa' + ab + a'b' + bb')' -- Distributive Law
F = (ab + a'b')' -- Complement Law
F = ((a' + b')' + (a + b)')' -- De Morgan's Theorem

Can now figure out delay from equation or draw design and find delay

5. Calculate Delay

Draw design and find delay

F = ((a' + b')' + (a + b)')'



Delay: 4.2 NS

6-10. VHDL Coding

Ready for Xilinx!

Summary

- Lab 1 methodology
- XOR gate example
  - Lab procedure walkthrough