CECS
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CECS Seminar

"DRAC: Designing RISC-V-based Accelerators for next generation Computers"

Miquel Moreto, Ph.D.

Ramon y Cajal Fellow at Universitat Politècnica de Catalunya (UPC) and Associate Researcher at BSC

Wednesday, August 10th
11:00 a.m. - 12:00 p.m. PST
Location: DBH 3011
Zoom Link

Abstract: Designing RISC-V-based Accelerators for next generation Computers (DRAC) is a 3-year project (2019-2022) funded by the ERDF Operational Program of Catalonia 2014-2020. DRAC will design, verify, implement and fabricate a high performance general purpose processor that will incorporate different accelerators based on the RISC-V technology, with specific applications in the field of post-quantum security, genomics and autonomous navigation. In this talk, we will provide an overview of the main achievements in the DRAC project, including the fabrication of Lagarto, the first RISC-V processor developed in Spain.

Biography: Miquel Moreto is a Ramon y Cajal Fellow at the Computer Architecture Departament (DAC) at the Universitat Politècnica de Catalunya (UPC), and he leads the High Performance Domain Specific Architectures team at the Barcelona Supercomputing Center (BSC). Miquel received his Ph.D. from UPC in 2010. After finishing the PhD, he spent 15 months at the International Computer Science Institute (ICSI), affiliated with UC Berkeley, as a Fulbright Postdoctoral Research Fellowship Holder during 2011 and 2012. In 2013, he returned to Barcelona to work on multiple European projects (RoMoL, Mont-Blanc, EPI, DeepHealth, eProcessor) and industrial projects (Arm, IBM, Lenovo). In 2019, he led the design and fabrication of Lagarto, the first processor developed in Spain based on the open source RISC-V instruction set architecture. Currently, he coordinates the DRAC project, which is promoting the Lagarto initiative with new generations of the Lagarto processor and accelerators.

Host: Prof. Veidenbaum