



**CECS**

**CENTER FOR EMBEDDED & CYBER-PHYSICAL SYSTEMS  
UNIVERSITY OF CALIFORNIA · IRVINE**

## CECS Seminar

*“Partial Logic Synthesis and its Application to automatic generation of parallel/distributed algorithms”*



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Thursday, January 17<sup>th</sup>  
3:00 p.m.  
Engineering Hall 3206

**Abstract:** In this talk first we review the partial logic synthesis problem and its associated algorithm based on QBF (Quantified Boolean Formula) formulation. Partial logic synthesis is to generate appropriate sub-circuits for the missing portions in the target design so that the entire circuit becomes equivalent to the specification which is separately given. Then we show the problem to automatically generate distributed/parallel computing for the given specification can be defined as partial logic synthesis problem. Taking matrix-vector product computation as an example, we show how theoretical optimum distributed/parallel computation can be automatically generated targeting many cores/chips which are connected through a ring connection.

**Biography:** Masahiro Fujita received his Ph.D. in Information Engineering from the University of Tokyo in 1985 on his work on model checking of hardware designs by using logic programming languages. In 1985, he joined Fujitsu as a researcher and started to work on hardware automatic synthesis as well as formal verification methods and tools, including enhancements of BDD/SAT-based techniques. Since March 2000, he has been a professor at VLSI Design and Education Center of the University of Tokyo. He has been involved in a Japanese governmental research project for dependable system designs and has developed a formal verifier for C programs that could be used for both hardware and embedded software designs. He has authored and co-authored 10 books, and has more than 200 publications.