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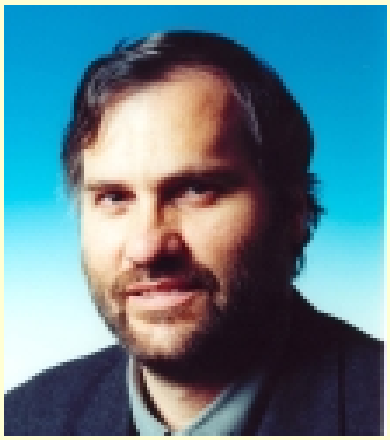
CECS Seminar Series 2018

"Near-Threshold Computing: The bottom floor for Energy in IoT devices and its Vanishing Design Noise Margins"



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Thursday, February 15 at 2:00-3:00PM

ICS 432

Abstract: Promising opportunities for research on heterogeneous Internet-of- Things (IoT) devices lie at the energy-bottom floor, where CMOS is still an unbeatable, flexible technology to make the internet of "everything" possible and cost-effective. Near-threshold computing (NTC) in CMOS is a promising alternative for any application which can tolerate or benefit from very wide voltage-frequency scaling (VFS). The digital blocks of devices may operate at very different power-performance modes, from sub-MHz to peaks of hundreds of MHz, which requires CMOS design libraries targeted for NTC. The analog and RF content on IoT chips will be even more crucial, from a power-savings standpoint. In IoT it is best to avoid using costlier CMOS, and yet closer to an end, two-dimensional transistor and IC scaling. The nano-power range which is achievable in deca-nanometer CMOS at near-VT requires very specific logic design techniques to be applied in digital CMOS. This talk addresses a method to design CMOS digital circuits for a wide dynamic range of VFS, and targets near-threshold for best energy-efficiency. Our work on 65nm CMOS has demonstrated 63X to 77X energy/operation savings for applications that tolerate ultra-wide frequency scaling (from hundreds of KHz to 1GHz) in their system operating modes. The results in CMOS were obtained using the minimal cycle time achievable at each supply voltage, down to very low 200 mV supplies. The strategy for transistor sizing in digital cells and static noise margin maximization will be addressed in particular. The seminar seeks to stimulate system-level and circuit-level design approaches for IoT nodes, as the presenter is available to discuss digital, mixed-signal, and even RF aspects of CMOS systems-on-IoT-devices.

Biography: Sergio Bampi received the B.Sc in Electronics Engineering and the B.Sc. in Physics from the Federal Univ. of Rio Grande do Sul (UFRGS, 1979), and the M.Sc. and Ph.D. degrees in EE from Stanford University (USA) in 1986. Full professor in the Digital Systems and Microelectronics design fields at the Informatics Institute, member of the faculty since 1986. He is a member of the PPGC Computing Graduate Program since 1988, and of the PGMICRO since its start in 2002. He served as Graduate Program Coordinator (2003-2007), head of research group and projects, technical director of the Microelectronics Center CEITEC (2005-2008) and is the past President of the FAPERGS Research Funding Foundation and of the SBMICRO Society (2002-2006). He is a former member of HP Inc. technical staff, and a visiting research faculty at Stanford University (1998-99). His research interests are in the area of IC design, nano-CMOS devices, mixed signal and RF CMOS design, ultra-low power digital design, dedicated complex algorithms, architectures, and ASICs for image and video processing. He has co-authored more than 360 papers in these fields and in MOS devices and EDA. He is a senior member of IEEE. He was Technical Program Chair of IEEE SBCCI Symposium (1997, 2005), SBMICRO (1989, 1995), IEEE LASCAS (2013), VARI 2016 Conferences and Workshops.