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CENTER FOR EMBEDDED & CYBER-PHYSICAL SYSTEMS

## CECS Seminar Series

*Presents*

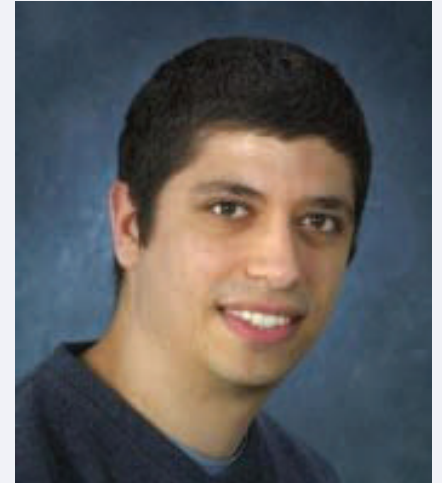
**“High Level Synthesis—Some Challenging Problems”**

**Wednesday, November 16th, 2016**

**11:00a.m. - 12:00p.m.**

**Engineering Hall 2430**

**Host: Professor Nikil Dutt**



**George A. Constantinides**  
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# UCIRVINE

**Abstract:** High Level Synthesis - synthesis of circuits from behavioural descriptions - is a long-standing problem, but one that appears to now have come of age. Both the demand for, and the supply of, quality HLS tools is now in place. However, there are still some hard problems to be overcome in order to make HLS fully general. My research focuses on two of these: customisation of memory systems to algorithms, and customisation of number representation to algorithms. After briefly introducing the work at Imperial - and encouraging PhD and postdoc applications (!) - I will spend a little time on each of these problems. In particular, I will look at the problem of customisation of memory for heap manipulating programs, the potential of parametric analysis for synthesis of lightweight run-time scheduling changes, and automated code refactoring for rigorously controlled accuracy / latency / area optimization. I hope to inspire the audience to consider how you may be able to contribute to these problems.

**Biography:** Prof George A. Constantinides holds the Royal Academy of Engineering / Imagination Technologies Chair in Digital Computation at Imperial College London, where he leads the Circuits and Systems research group. He has been a member of staff at Imperial since 2001. Over this time he has been the proud supervisor of 25 graduated PhD students and chaired the FPGA, FPT and FPL conferences. He enjoys hard problems and espresso.