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Present

Area/speed tradeoffs in a retargetable FPGA-optimized processor core

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Abstract

Can portable yet efficient, FPGA-optimized processor cores be constructed using generic HDL, without depending on any vendor-specific primitives? In this talk we will discuss the techniques applied for achieving a balance between instruction throughput and FPGA resource utilization in a synthesizable scalar core which outperforms its proprietary counterparts (MicroBlaze, Nios, Cortex-M3) by 20% to 40% in industry-standard integer benchmarks (CoreMark, Dhrystone per MHz) while occupying less than 1000 6-input LUTs, and less than 650 LUTs in an area-optimized configuration. The core can be retargeted to execute subsets of either the emerging RISC-V or the traditional MIPS instruction sets, and is supported by contemporary GNU-based software toolchains.

Biography

Marko Zec received a BSc in electrical engineering from the University of Zagreb, where since 2005. he has been working as a project scientist on various computer networks projects with funding from ICSI Berkeley, the FreeBSD foundation, Boeing Integrated Defense Systems, and Ericsson. His research interests include operating systems, computer networks, software-based packet processing datapaths, and programmable logic.

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CECS Conference Room
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