CECS

CENTER FOR EMBEDDED & CYBER-PHYSICAL SYSTEMS

CECS Seminar Series

Present

"Flexible-Stretchable-Reconfigurable CMOS Electronics Through Hybrid Integration of Heterogeneous Materials for Wearable Interactive Electronic Systems"

Professor Muhammad Mustafa Hussain

King Abdullah University of Science and Technology (KAUST)

Abstract: Our research is focused on heterogeneous electronic materials and high-performance complementary metal oxide semiconductor (CMOS) based tunable shape-size-conformity wearable interactive electronics and systems for smart living (computation-communication-infotainment) through internet of everything and a sustainable future (healthcare-water-food-environment-security). For scientific exploration, we make collective use of the materials, processes and device architecture leveraging multidisciplinary tracks of material science, bioengineering, mechanical, environmental engineering and computer science. As engineering tool, we use CMOS technology extensively due to its industrial relevance, maturity and reliability for rapid tech transfer.

To bridge between the high-performance state-of-the-art electronics and emerging soft-materials based flexible-stretchable electronics. we have developed various generic batch processes using CMOS technologies to transform any already processed Integrated Circuitry (IC) or arrays of devices to be fabricated on virgin substrates (thin film based, examples include but not limited to: silicon, silicon germanium, indium phosphide, gallium arsenide, etc.) into flexible and stretchable one [ACS Nano 2014, pss-RRL 2014]. These processes are cost effective ($1.25/cm2), non-abrasive and retain high-performance, energy-efficiency, ultra-large-scale-integration density as obtained in today's state-of-the-art electronics. Often the transformed fabrics (ultra-thin version of the bulk thin film substrates with pre-fabricated devices) are semi-transparent due to the presence of the process originated vertical channels. As per ITRS 2014 metrics, the processes are fully scalable down to 2 nm technology node. Using these techniques we have demonstrated high-κ/metal gate based planar and non-planar nano-scale (sub-20 nm) CMOS logic devices [Adv. Mater. 2014 (cover page), ACS Nano 2014, APL 2013, pss-RRL 2013 (cover pages), IEEE TED 2013, pss-RRL 2013, Sci. Rep. 2013, pss-RRL 2013], memory [Adv. Electronic Mater. 2015, Microelect. Engr. 2014], micro-scale thermoelectric generators [Small 2013 (frontispiece)], micro lithium ion batteries (150 µAh/cm2 normalized capacity), MEMS devices [MEMS 2014], smart thermal patch using copper stretched up to 800% [Adv. Healthcare Mater. 2015 (frontispiece)], mono-crystalline silicon stretched up to 1000% [APL 2014]. Variety of device demonstrations on wide range of inorganic thin films using this technique proves the efficiency and versatility of it. Our research greatly complements the $150M Flexible Hybrid Electronics Manufacturing Initiative (FHEMII) – recently introduced by the US Department of Defense: "Highly tailorable devices on flexible, stretchable substrates that combined thinned CMOS components with components that are added via printing process".

Biography: Dr. Muhammad Mustafa Hussain (PhD, ECE, UT Austin, Dec 2005) before joining KAUST was Program Manager of Emerging Technology Program in SEMATECH, Austin. His program was funded by DARPA NEMS, CERA and STEEP programs. A regular panelist of US NSF grants reviewing committees, Dr. Hussain is the Editor-in-Chief of Applied Nanoscience (Springer) and an IEEE Senior Member. He has served as first or corresponding author in 70% of his 202 research papers (including 12 cover articles and 82 journal papers). He has 15 issued and pending US patents. His students are working in UC Berkeley, UIUC, UC-Davis and in DOW Chemicals. Scientific American has listed his research as one of the Top 10 World Changing Ideas 2014.

Tuesday, July 14, 2015 - 11:00 a.m.

Donald Bren Hall 3011

Host: Professor Nikil Dutt

UNIVERSITY OF CALIFORNIA, IRVINE