Date/Time: Monday, June 24th, 2013, 1:00 p.m.
Location: Engineering Hall, Room 2210

Committee Members:
Shinozuka Masanobu (Chair)
Ian Harris
Pai Chou

Abstract:
Sensing systems often require data logging to local flash-memory storage to reduce data transmission bandwidth and power requirements. Unfortunately, the necessity of low- power consumption and the inherent bottlenecks of said low-power hardware input/output (I/O) architecture make it difficult to achieve the required data-logging performance on conventional sensor platforms, even when using direct-memory access (DMA). To address this problem, we propose a new, high-performance, low-power hybrid FRAM/flash storage interface module that can connect mass storage devices to a vast majority of modern mi- crocontroller units (MCU) via the ubiquitous serial peripheral interface (SPI). It consists of high-speed, low-power FRAM buffers to facilitate data transfers and file-system metadata caching, along with proven high-speed data-handling techniques such as data striping. A small but effective master-slave bus controller eliminates the I/O bottleneck by enabling direct slave-to-slave communication of sensor devices to the storage module and simultaneous buffering and flushing of data, thereby cutting the total number of transactions in half without having to increase bus clock speed or to allocate extra amount of resources such as internal SRAM space and DMA channels to increase transfer speed. Experimental results show that our proposed storage interface increased the I/O performance by 74% while yielding a 75% energy savings over conventional sensor logging systems, all without sacrificing additional resources of the microprocessor. The proposed architecture is not limited to just benefitting storage systems, but also contribute to microprocessors with new paradigms for efficient data transactions.