



CECS Seminar Series

“Evaluating GALS Systems for System Integration-Outlook and Future Prospects”

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Abstract

Globally Asynchronous Locally Synchronous (GALS) methodology has been proposed already in 90's as a solution for complex system integration. This methodology has been widely investigated by academia, and several solutions started to appear also in commercial solutions. In this talk we will present the recent results about the GALS methodology validation and characterization. Additionally, the overall state-of-the-art of the system integration with GALS will be presented. GALS is technology today frequently used in the physical layer of Network on Chip interconnect, delivering new architectures of a network switch and network adapter. Various research groups have confirmed the advantages of GALS technique for increasing the system modularity and reducing the challenges of global clock distribution.

In addition to that, the result of IHP's GALS group will be presented, that are focused on additional benefits from GALS technique on the system level. In particular it will be evaluated low-EMI and switching noise features of GALS technique, which are extremely important for complex implementations in scaled technologies and mixed SoC designs. The achieved results measured on complex CMOS chip named Moonrake in the scaled 40 nm CMOS process showed that EMI reduction of up to 26 dB could be achieved using GALS

Finally the prospects of the future use of GALS technology will be introduced. The focus of this elaboration will be the application of GALS technique for secure energy efficient wireless sensor nodes. In this context the possibilities for energy reduction and compatibility to the main power optimization flows will be analysed.

Biography

Milos Krstic received his M.Sc. degree in Electrical Engineering at Faculty of Electronic Eng. Nis, Serbia in 2001, and his Dr.-Ing. degree from the Brandenburg University of Technology, Cottbus, Germany in 2006. Since 2001 he has been with IHP Microelectronics, Frankfurt (Oder), Germany, in the Wireless Communication Systems Department. For the last few years, his work was mainly focused on low power digital design for wireless applications and globally-asynchronous locally-synchronous (GALS) methodologies for digital systems integration. Since 2010 he has taken over the position of team leader of the group for Design & Test methodology in IHP that includes 15 researchers and test engineers. He was coordinating EU project GALAXY on GALS methodology for system integration, and now leads various projects in the area of GALS design, switching noise reduction techniques, radhard and fault tolerant design for space applications. His academic and professional work was followed with more than 70 journal and conference papers and 9 submitted patent applications (5 registered patents).

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2:00PM-3:00PM

4011 Donald Bren Hall

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