Self-Timed Circuits for Energy Harvesting AC Power Supplies

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ABSTRACT

The recent explosion in capability of embedded and portable electronics has not been matched by battery technology. The slow growth of battery energy density has limited device lifetime and added weight and volume. Passive energy harvesting from vibration has potentially wide application in wearable and embedded sensors to complement or replace batteries. We propose increasing energy harvesting efficiency by eliminating AC/DC conversion electronics. We investigated self-timed circuits, power-on-reset circuitry and memory for energy harvesting AC power supplies. Our power-on-reset circuit achieves a substantial improvement over conventional approaches with 4.1 nW of simulated power dissipation and frequency-independent turn-on voltage. A chip is being fabricated to test the circuits presented here.

Categories and Subject Descriptors: B.7 Hardware: Integrated Circuits

General Terms: Design

Keywords: energy harvesting, self-timed circuits, AC power supplies, dynamic memory, power-on-reset

1. INTRODUCTION

Over the past decade, the number and variety of embedded digital electronics has exploded, driven by applications such as cellular phones, portable multimedia devices, and sensor networks. Yet this dramatic increase in functionality and computing power has not been matched by slowly improving battery technology. Energy harvesting from environmental sources is a promising alternative which can reduce system weight and volume, increase operating lifetime, decrease maintenance costs, and open new frontiers for integrating digital computation with sensing and actuation.

Because communication typically consumes much more power than computation, many applications want to maximize the amount of computation done at a particular sensor network node [1]. Off-chip power electronics increase system cost and volume and limit energy harvesting operation due to losses in the conversion from AC to DC voltage. Recent projects, summarized in Table 1, have shown poor efficiencies for energy harvesting power electronics. Much current work is addressing these problems from the power generation side by developing and optimizing transducers for energy harvesting. However, the desire for smaller devices and higher levels of integration fundamentally limit output power.

The work presented here addresses these issues from the power consumption standpoint. By interfacing digital circuits directly to the AC output of an energy harvester, the power dissipation and cost of complex power electronics can be avoided. Significant digital computation can still be completed with the AC power supply because the supply frequency is several orders of magnitude lower than the integrated circuit operation frequency. For each power supply cycle, the chip must turn on, perform computation, and turn off. To guarantee correct operation, an accurate power-on-reset circuit is needed to properly initialize the chip at the beginning of every power supply cycle. The power-on-reset circuit should also set an enable signal that controls when circuit operation starts. After a reset pulse occurs, the circuits must operate correctly over large variation in the supply voltage. Self-timed circuit design is used because it is robust to parameter variations, including supply voltage [2].

Between every power supply cycle, the supply voltage reaches a minimum and any finite state machines and pipeline registers potentially lose state. A dynamic memory cell optimized to store data over short periods without a power supply can enable continuous computation by preserving states between power supply cycles.

This paper proposes a digital system that combines a novel power-on-reset circuit, self-timed circuit design, and dynamic memory using vibration-based energy harvesters as an AC power supply. A chip is currently being fabricated to test the circuits presented here.

2. ENERGY HARVESTERS

Vibration-based energy harvesters consist of a mechanical element that moves in response to external vibrations and a coupling mechanism that converts mechanical movement into electrical energy. The mechanical response can be modeled as a damped-driven oscillator with behavior described

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Energy Harvesting Method	Implementation (Previously Reported)	Total Power Output	Power Electronics Load	Efficiency
Electromagnetic Moving Coil	Amirtharajah [3]	18 μW	13.2 μW	26 %
MEMS Variable Capacitor	Meninger [4]	8.7 μW	4.4 μW	49 %
	Mur Miranda [5]	61 μW	28 μW	46 %
Piezoelectric (Vibrations)	Roundy [6]	375 μW	190 μW	50 %
	Ottman [7]	12.9 mW	4.5 mW	65 %
Piezoelectric (Shoe Inserts)	Schenck [8]	8.4 mW	6.9 mW	18 %

Table 1: Recent energy harvesting projects and associated power electronics efficiency

as $m\ddot{z} + b_m\dot{z} + kz = -m\ddot{y}$, where z and y represent position of the harvester mass and base, respectively, b_m is the mechanical damping coefficient, k is the spring constant, and m is the mass. The electrical circuit is generally modeled as a damping term in parallel with the mechanical damping [9].

There are three main types of vibration-based energy harvesters. Electromagnetic converters generate a voltage by moving a coil relative to a fixed magnetic field [10]. Electrostatic converters place charge onto a variable capacitor and allow the vibrations to move the capacitor plates apart, reducing the capacitance. Capacitance and charge are related as $Q = CV$, so if Q is fixed and C decreases, V must increase [4] [9]. Piezoelectric generators use a piezo beam mounted as a cantilever with a mass on the unsupported end. Electrodes are plated on surfaces of the beam and sometimes between layers of the piezo material. As the beam flexes, a potential difference is created between the electrodes [11].

Several recent papers describe the theoretical and measured power output from various vibration-based energy scavenging devices. Figure 1 summarizes these published results [4] [9] [10] [12]. If the power results are restricted to only measured values from average amplitude vibrations, then power on the order of 100 μW is expected. The mechanical vibrations are expected to have frequencies between 60 Hz and 1 kHz and vibration amplitudes between 2.5 μm and 5 μm.

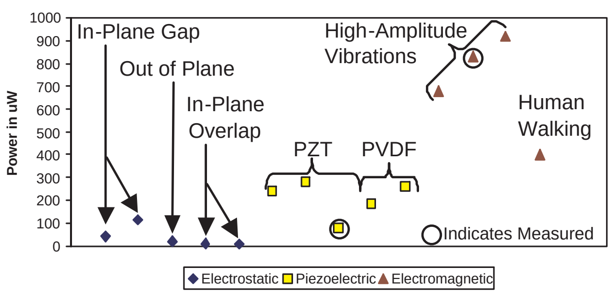

Figure 1: Harvester output powers

3. SELF-TIMING FOR AC SUPPLIES

3.1 Power-On-Reset Circuit

A power-on-reset circuit for AC supplies ideally has a turn-on voltage in the deep subthreshold region. This maximizes the fraction of the power supply cycle during which the circuit is operating while minimizing power dissipation. In order to function correctly with a low turn-on voltage over the target range of frequencies, the power-on-reset circuit must generate a reset pulse independent of power supply frequency. Conventional power-on-reset circuits typically use an RC charging delay to at least partially control the turn-on voltage [13]. To design a power-on-reset circuit suitable for AC power supplies, a different approach was taken.

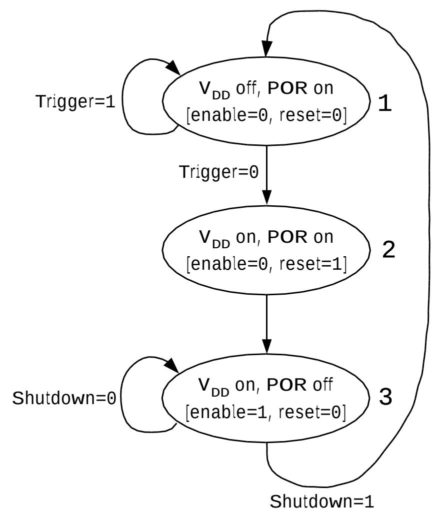

Figure 2: Power-on-reset state diagram

At a high level, the circuit functions as an analog finite state machine (FSM). The reasons for calling this circuit an analog FSM are that it has no clock signal and the state variables are analog signals (capacitor voltages). State transitions are triggered by analog sense circuits. Consider the state diagram in Figure 2. V_{DD} and a power-on-reset (POR) enable signal are analog state variables that identify three different states. The circuit shown in Figure 3 implements this sequence of states. State 1 (V_{DD} off, POR on) corresponds to the beginning of a power supply cycle. The FSM waits in this state until the voltage threshold detector indicates that V_{DD} has risen above some threshold by lowering the trigger signal. When in state 2 (V_{DD} on, POR on), the power supply is considered on, therefore reset is asserted. Next, enable is asserted, the POR circuit turns off, and the FSM transitions into state 3 (V_{DD} on, POR off). This state represents the normal operating condition for the chip. A reset circuit asserts the shutdown signal when V_{DD} turns off, causing the enable signal to go low and reinitializing the POR circuit for the next power supply cycle.

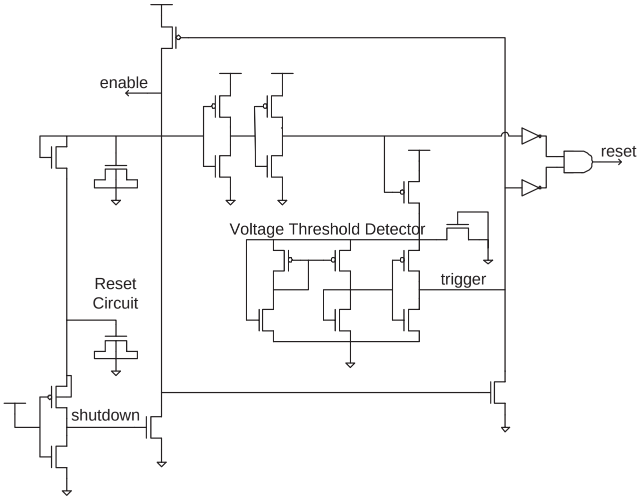

Figure 3: Power-on-reset circuit

The power-on-reset circuit was simulated using a post-layout extracted netlist in Spectre. Table 2 summarizes the power-on-reset performance. Figure 4 shows the turn-on voltage over the full operating range of temperature, frequency, and process variation.

	Avg.	Max.	Min.
Turn-on voltage	0.45 V	0.61 V	0.30 V
Average power	4.1 nW	40.9 nW	0.1 nW
Peak power	500 nW	4.32 μW	7.5 nW

Table 2: Power-on-reset performance

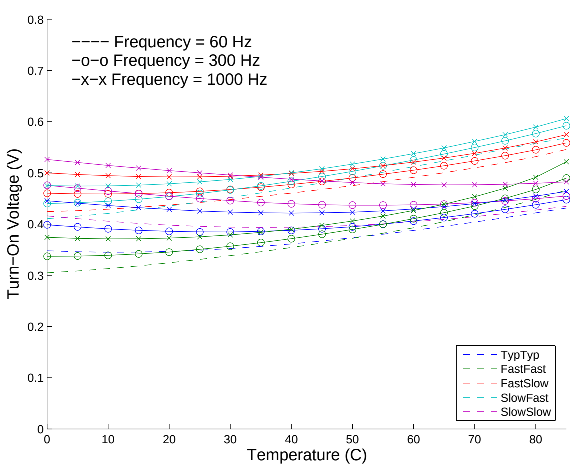

Figure 4: Power-on-reset turn-on voltage

3.2 Ring Oscillator Self-Timed Circuit

Figure 5 shows a self-timed pipelined datapath in which the clock is provided by a ring oscillator containing a replica of the critical path [2]. This design style is similar to traditional synchronous design in that the worst case performance of the longest pipe stage delay dictates frequency of operation. The ring oscillator frequency, however, varies with supply, temperature, and process automatically to ensure correct operation. Robustness to voltage and temperature was demonstrated in simulation using a self-timed clock for a distributed arithmetic unit with 16-bit ripple carry adders [10]. A replica of the adder critical path forms the ring oscillator. Performance of the self-timed datapath degrades as supply voltage is reduced, but the datapath still operates correctly.

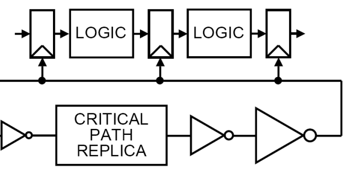

Figure 5: Self-timed datapath

The self-timed datapath and power-on-reset circuit can also operate correctly under a DC supply voltage. In this situation, the power-on-reset circuit will produce a reset pulse during the supply voltage rise time. The self-timed ring oscillator matches the clock frequency to the constant supply voltage and the chip operates as a traditional DC supply system. This provides the potential for a dual-supply system where energy can be harvested from multiple ambient energy sources.

4. MEMORY FOR AC SUPPLIES

The combination of an AC power supply and a small power budget place strict limits on the types of memory that can be used for this system. Memory cells must be able to hold their values while the power supply is too low to operate without requiring frequent refreshing. Circuits requiring DC bias current must be eliminated. Due to these concerns, a three-transistor DRAM cell with non-destructive read was selected [14]. The sensing circuit for this cell is built from two transmission gates, a precharge transistor, and a tristate buffer. The memory cell and its sensing circuit are shown in Figure 6 where transistors M1, M2, and M3 make up the memory cell.

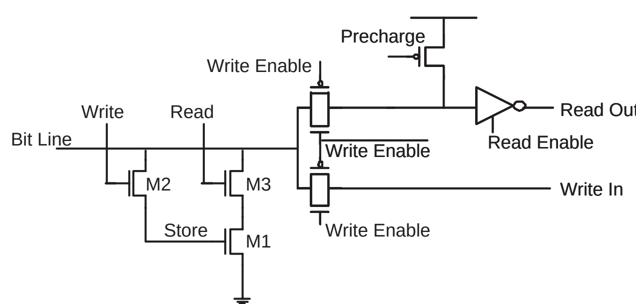

Figure 6: DRAM cell and sense circuit

The gate of transistor M1 and the source diffusion of transistor M2 comprise the storage node capacitance. Transistor M1 is sized to have a length of 9.9 μm and a width of 4.59 μm. Write transistor M2 is minimum sized. Simulations indicate that this configuration has the best ability to both minimize leakage and maximize the peak voltage written to the storage node. The storage node has approximately 300 fF of capacitance and is able to hold its state correctly for at least 1.2 ms, the time where the supply voltage is too low to operate for a rectified 60 Hz supply.

These memory cells were used to build two 16×16 memory arrays on the test chip currently being fabricated. On receiving a reset pulse from the power-on-reset circuit or a refresh pulse from an internal timer, the DRAM controller cycles through the memory array, reading and then re-writing each 16-cell row.

5. CONCLUSIONS AND FUTURE WORK

A chip to test these proposed circuits for energy harvesting applications was designed in a 0.18 μm logic process. A simplified block diagram of the test chip is shown in Figure 7. The chip uses a scalable resolution FIR filter using distributed arithmetic as a test structure [10] and is currently being fabricated.

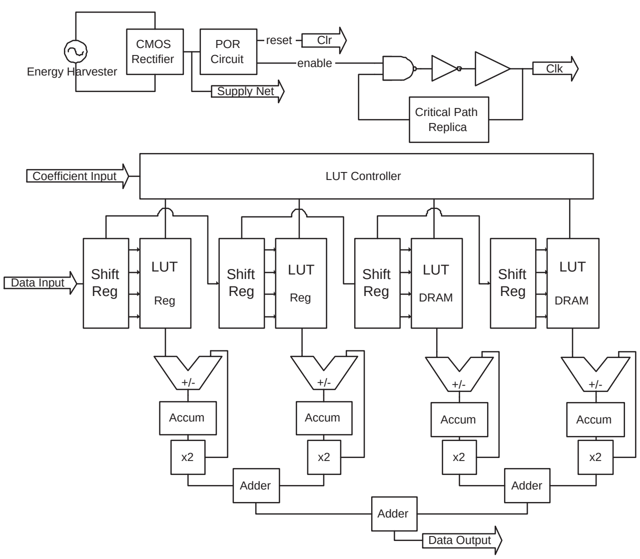

Figure 7: Test chip block diagram

These circuits can be generalized to interface with inductively powered devices, a growing area with applications such as biomedical implants, embedded sensors, and RFID tags [15]. The proposed power-on-reset circuit was designed for low frequency power supplies but could be adapted for these higher frequency applications. The current design achieves correct operation in simulation up to a supply frequency of 250 kHz over all process corners and temperatures below $50^{\circ}C$.

Analog circuits should also be included in a full system. To function, analog circuits would require a high power supply rejection ratio and a bias that stabilizes quickly, possibly by exploiting a digital preset on initialization. If these needs were met, analog circuits should be able to work properly over short time periods in the supply cycle. The combination of analog and digital circuits which can operate on an AC supply from an energy harvester opens the door for full mixed-signal, system-on-chip implementations for wireless sensor networks.

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