Yield Prediction for 3D Capacitive Interconnections

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ABSTRACT

Capacitive interconnections are very promising structures for high-speed and low-power signaling in 3D packages. Since the performance of AC links, in terms of Band-Width and Bit-Error-Rate (BER), depends on assembly and synchronization accuracy we performed a statistical analysis of assembly procedures and communication circuits. In this paper we present a yield prediction methodology for 3D capacitive links: starting from the analysis of communication circuits and BER measurements, we analyze stacking variability in order to predict reliability and performance. The proposed parametric yield analysis is demonstrated on a test-case, with constrained inter-electrode coupling and operating frequency.

1. INTRODUCTION

Three dimensional (3D) integration is a very promising technology for the effective integration of complex systems: devices that are optimally implemented with various different technologies can be separately manufactured and then stacked and connected by means of efficient vertical interconnections over a very short range; this provides most of the benefits of on-chip integration while leveraging the yield improvement and manufacturing capability of separate components. Many solutions have been presented for the realization of 3D systems, such as System-in-Package, Through Substrate VIAs and wireless interconnections. This last approach provides a compelling integration paradigm: standard manufactured chips can be assembled using standard packaging procedures; moreover, the contactless approach naturally copes with many integration issues, such as ESD protection and the direct connection between circuits belonging to different power domains or realized using different materials. In the last few years, several prototypes have been presented demonstrating capacitive [6, 7, 1] and inductive [3, 5, 4] signaling with Gbps bandwidth and low power consumption. In this work we focus on 3D capacitive interconnections, where chips are stacked and aligned face-to-face with electrodes that provide the capacitive coupling exploited by communication circuits (Fig. 1). Our experience with this technology includes a 900Mbps/pin bandwidth solution with electrodes down to 8x8μm^2 [1]. Since the yield of finished packages is strongly related to communication quality and this is a key issue in making 3D capacitive interconnection a main-stream assembly technology, we here present for the first time a study of contactless communication in terms of process variability.

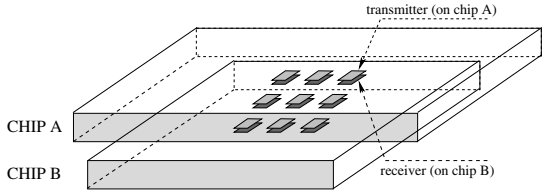

Figure 1: Capacitive interconnection concept.

We first analyze the interconnection behavior using a semi-empirical interconnection model: Bit-Error-Rate (BER) measurements are fitted by the analytical description of the communication circuits. We then use a parametric yield analysis methodology in order to study reliability and performance of the AC interconnections [8]: the former refers to the probability that the capacitive coupling is so poor that interconnection is not reliable; the latter takes into consideration the effects of stacking parameters on delays along the vertical paths. To compute the parametric yield as a function of these delays, a statistical timing analysis method [9, 10] is applied and a complete physical characterization of capacitive interconnections carried out.

The paper is organized as follows: in Section 2, we provide a brief overview of 3D technologies; in Section 3, the communication circuits are described; in Section 4, BER measurements are reviewed and fitted; in Section 5, we examine the assembly procedure and its variability; finally, we perform reliability (Section 6) and timing analysis (Section 7) and we present the conclusions (Section 8).

2. CONTACTLESS 3D TECHNOLOGIES

Three-dimensional integration technologies play an essential role in preventing some of the pains of deep sub-micron (DSM) integration [12, 13, 14]. The advantages of this approach are manifold:

- Efficient 3D interconnections can be allocated over the entire surface of a chip, providing an extremely wide communication parallelism;

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- Dies manufactured in different technologies can be assembled within the same package so that each part of the system can be implemented by using the most appropriate fabrication flow;

- Logic can be partitioned in different chips so that denser and shorter routing can also be achieved.

Many 3D fabrication flows have been investigated in recent years, differing in *method of assembly, number of layers available, impact on system geometry* and *related parasitic load* [11]. In this paper we focus on contactless connectivity.

For this approach, the communication is based on inductive [3, 5, 4] or capacitive [6, 7, 1] coupling between receivers and transmitters belonging to different chips. The inductive-based solution allows the connection of more than two layers (stacked face-to-back) within the same package, but requires a large pitch as well as high power consumption. For capacitive communication (Fig. 1), receivers and transmitters are implemented on each device and are coupled by capacitive electrodes, realized in the upper metal layer; in this case, chips are stacked face-to-face. Capacitive communication provides high bandwidth (over 900Mbps/pin with electrodes down to 8x8μm^2, 14$Mbps/\mu m^2$) as well as very low power consumption (0.14$mW/Gbps$) [1]. We proved the functionality of these interconnections for a chip-level assembly procedure [1] as well as for a wafer-level one [2].

Capacitive interconnections show a number of advantages with respect to other 3D technologies. No modification to the manufacturing process is required and assembly can be performed at die-level, so that chips can be verified before assembly. AC interconnections are more reliable than DC ones, which suffer from mechanical stress. There is much less parasitic load than with bonding wires or micro-bumps and ESD protections are not required. Moreover, wireless communication automatically figures out many issues about heterogeneous integration: since no contact is present, properly designed communication circuits naturally translate the DC components between different power domains and the absence of a direct connection avoids compatibility issues between different materials. Finally, since the connection mainly depends on communication circuits, capacitive links scale down with the technology node.

In comparison with common 3D options, the results reviewed in [1] show a performance that surpasses System-in-Package based on wire-bonding or micro-bumps, though with a still comparable assembly effort. With respect to through VIAs technologies, the interconnection pitch is increased, but the assembly process is far more simple and does not affect the silicon substrates. For all these reasons, capacitive interconnections are a very cost-effective option for the realization of 3D digital systems.

3. INTERCONNECT ANALYSIS

The communication circuits for capacitive interconnects [1] are shown in Fig. 2. The transmitter cell samples data for transmission and performs a level-to-edge encoding: on the rising edge of the TX clock, the input signal is sampled and propagated to the transmitter output; on the falling edge, the electrode switches to the inverted value performing the mentioned conversion. The receiver cell biases the receiver node in the high-gain state and samples the data received: during the high phase of the receiver clock, a CMOS switch

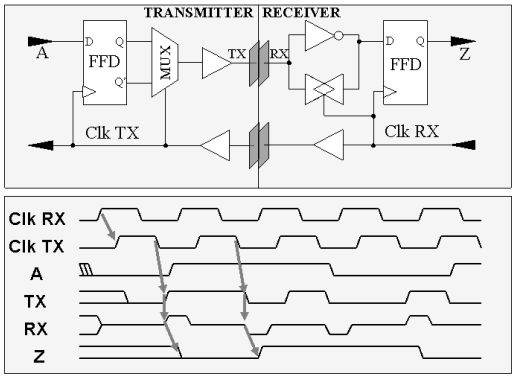

Figure 2: Circuits for AC interconnections.

biases the electrode on the logic-threshold of the input inverter; during the low phase of the clock, the electrode is left in a high-impedance state, ready to amplify the transmitted signal. Synchronization between receiver and transmitter is provided by a clock signal propagated from the receiver chip to the transmitter one; one single clock interconnection is used to synchronize a large number of data connections. The whole functionality is summarized in Fig. 2.

For the interconnect to work properly, three conditions must be satisfied:

- Sufficient inter-electrode coupling:

$$\Delta V_{RX} = \frac{C_{3D}}{C_{3D} + C_{GND}} V_{DD} > V_m \quad (1)$$

  where C_{3D} is the capacitive coupling between electrodes, C_{GND} is the parasitic capacitance on the receiver electrode and V_m represents the noise immunity margin;

- Timing margins for correct sampling of the received signal:

$$\Delta T_{TX} = (1-\delta)T - T_{D,TX} - T_{CLK,F} - T_{SU} > T_{TX,m} \quad (2)$$

  where $T_{D,TX}$ represents the data delay from the falling edge of transmitter clock to the input of receiver flip-flop, T_{CLK} is the skew between transmitter and receiver clock (respectively R for the rising edge or F for the falling one), δ is the clock duty-cycle and $T_{TX,m}$ represents an additional timing margin;

- Synchronization margins for the precharge-transmission phases:

$$\Delta T_{PRESET} = \delta T - T_{D,PRE} - T_{CLK,R} > T_{PRE,m} \quad (3)$$

  where $T_{D,PRE}$ represents the data delay from the rising edge of the same clock to the transmitter electrode (required during preset); $T_{PRE,m}$ is introduced as additional timing margin.

These conditions are the basis for both the Bit-Error-Rate model and the parametric yield one.

4. BIT-ERROR-RATE MODEL

To validate the communication approach, test-chips have been manufactured in 0.13μm technology ($V_{DD} = 1.2V$)

and assembled face-to-face [1]. The design includes a dedicated test interface, enabling testing-at-speed of the capacitive interconnection. Test-patterns are provided from an acquisition-board which performs the BER measurement as well. Fig. 3 presents the measured Bit-Error-Rate for 8x8μm^2 and 15x15μm^2 capacitive interconnects as well as the values predicted by the model we propose. The plots of the BER vs. frequency clearly show essentially no error on more than 10^{+13} measurements in a wide frequency spectrum; moreover, the BER is different in the case of transmitting a '0' or a '1' and it increases orders of magnitude in the range of a few MHz. Our model will reflect these observations. First, since condition (1) is frequency-independent[1], it does not contribute to the measured BER of the interconnections under-test.

Assuming that $T_{TX,m}$ and $T_{PRE,m}$ are stochastic variables with Gaussian distributed zero mean uncertainties, the probability that conditions (2) and (3) are met can be calculated as $P = 1 - 0.5erfc(\Delta T/\sigma\sqrt{2})$ where ΔT is the required value, and σ is the standard deviation. To compute a first-order BER model, the following definitions of error-probability are used:

$$EP_{tx} = \frac{1}{2} erfc\left(\frac{\Delta T_{TX}}{\sigma_{tx}\sqrt{2}}\right); \quad (4)$$

$$EP_{pre} = \frac{1}{2} erfc\left(\frac{\Delta T_{PRESET}}{\sigma_{preset}\sqrt{2}}\right); \quad (5)$$

Condition (3) yields soft-errors when the transmitted bit is equal to the previous one, since in this case the preset phase of transmitter is required. The error-probability due to condition (2) applies to each transmission, since it represents the arrival constraints required for data sampling. Assuming total correlations between the source of uncertainty, our first order BER model is:

$$BER = BER_{switch} + BER_{const},$$

where

$$BER_{switch} = P_{switch} EP_{tx};$$

$$BER_{const} = P_{const} MAX(EP_{tx}, EP_{pre});$$

where $P_{switch} = P(A[nT] \neq A[(n-1)T])$ and $P_{const} = P(A[nT] = A[(n-1)T])$; A is the transmitter input.

The propagation delays in (2-3) are obtained by nominal SPICE simulations. The timing uncertainties and duty-cycles in (4-5) are numerically computed to optimize the fit of the model with the measured data. Since propagation delay significantly differs for transmission of a '0' or a '1', the model takes the two cases into consideration separately; the fitted model is shown in Fig. 3 for 8x8μm^2 and 15x15μm^2 interconnections.

The BER model, together with the measured data, shows that BER is of little concern for the 3D capacitive interconnect scheme: a BER-aware design can improve working frequency of just few MHz.

5. PARAMETRIC YIELD AND ASSEMBLY VARIABILITY

[1]Resistance and inductance of the interconnect are negligible; for this reason, the inter-electrode transfer function is a constant capacitance ratio.

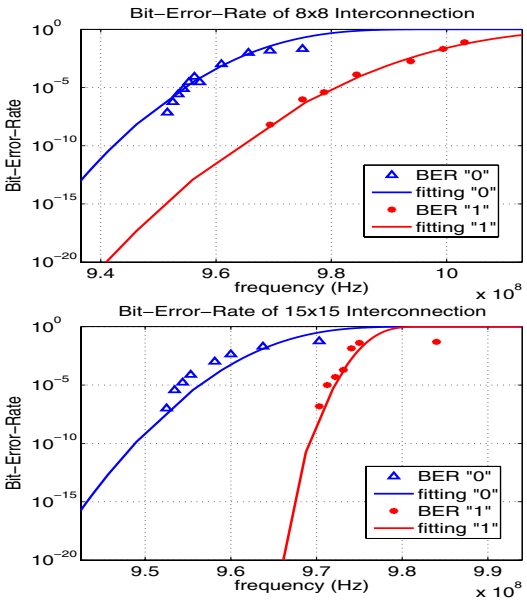

Figure 3: Measured BER and model fitting for 8x8 and 15x15 interconnections.

The actual number of samples we have access to and the relative maturity of the technology do not allow for any meaningful statistical analysis of catastrophic yield; we thus focus on parametric yield, as this can be estimated by using mathematical modeling and simulations. Parametric yield is particularly important at this early stage of the technology since it can provide a design guideline not only for circuit implementation but also for assembly development. The yield model we propose consists of two parts: the first part, which refers to interconnect reliability (Y_R), is the probability of meeting the capacitance constraint that is required by condition (1); the second part, which refers to interconnect performance (Y_T), is the probability that the timing constraints expressed in conditions (2-3) are satisfied.

In this analysis, we only consider the statistical variations that affect 3D capacitive coupling and that depend on the assembly technology. There are two main assembly parameters[2]:

- *Alignment accuracy.* The alignment variability primarily depends on the accuracy of the flip-chip bonder which provides an accuracy of $1\mu m$, with Gaussian distributed uncertainties.

- *Thickness of inter-chip dielectric.* The present number of available samples does not allow for any statistical characterization of dielectric thickness. Nevertheless, we can extract corner-case conditions, with best and worst cases at $0.5\mu m$ and $1.1\mu m$ respectively (sample-to-sample variations). We assume a Gaussian distribution, with $\pm 3\sigma$ corresponding to the corners.

Now, the distributions of interconnection capacitance can be inferred by running Monte Carlo (MC) analysis; they will then be used in order to analyze conditions (1-3). In

[2]These parameters are referred to [1] and they would get improved in future implementations.

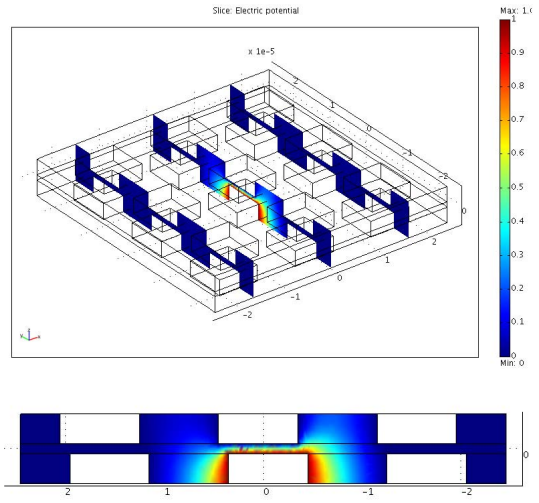

Figure 4: Physical model for parasitic extraction.

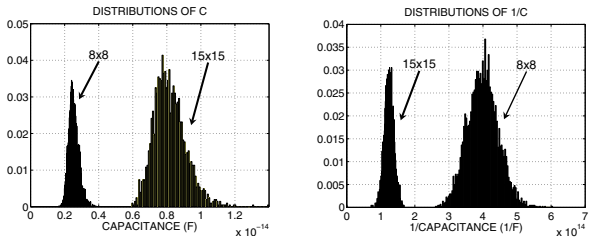

Figure 5: Capacitance Distributions for 8x8μm and 15x15μm electrodes.

order to compute the capacitances related to the chip stack, various different electrode geometries have been described using the FEMLAB® and MATLAB® environments [16, 15]; Fig. 4 shows a 3x3 array of interconnections. The mentioned structures describe the upper metal layer of each chip, in which the electrodes are implemented. Since the chips are not passivated, the electrodes are fully embedded in the adhesive layer. In order to perform Monte Carlo analysis, the geometries are fully parametric: size, pitch and thickness of electrodes, inter-chip distance, adhesive parameters and misalignment can be specified at execution time, enabling all design and stacking parameters to be evaluated. In order to speed-up the analysis, we use a 3x3 geometry for the evaluation of interconnection cross-talk, in nominal conditions, and a single-channel structure for the statistical analysis (extraction times are summarized in Table 3). This is possible because in our test-case cross-talk parasitics are two orders of magnitude smaller than inter-electrode coupling.

The capacitance distributions for 8x8μm^2 and 15x15μm^2 interconnections are presented in Fig. 5 as well as the distributions of $1/C_{3D}$; mean and standard deviations are summarized in Table 1. Since the relation between stacking parameters and capacitance is non linear, the resulting distributions are not exactly normal. Nevertheless, the distributions of $1/C_{3D}$ are very close to a Gaussian trend, because the adhesive thickness is the main source of variation. This approximation will be used in the discussion that follows in order to provide a direct calculation of parametric yield.

	8x8μm^2	15x15μm^2	25x25μm^2
$\overline{C_{3D}}(fF)$	2.53	8.17	21.5fF
$\sigma_C(fF)$	0.3	0.99	2.1
$\overline{C_{3D}^{-1}}(F^{-1})$	3.99E+14	1.23E+14	4.56E+13
$\sigma_{C^{-1}}(F^{-1})$	0.45E+14	0.13E+14	0.9E+13
C_{3D} min.	2.2fF	3fF	5.5fF
$1-Y_R$	0.116	≤1E-50	≤1E-50

Table 1: Coupling Variation and Fault Probability.

6. RELIABILITY OF CAPACITIVE INTERCONNECTIONS

Condition (1) determines the minimum coupling requirements for one to have a functional interconnect: if the propagated voltage is low, the noise sensitivity is increased and the capacitive interconnection becomes unreliable, even at low frequency. In order to perform this analysis, the voltage constraint will be defined as $V_m = V_{DD}/2 - V_t$: if this condition is respected, the receiver input reaches the low-gain region after each transmission and the sensitivity to noise is very low. In order to translate voltage constraints into minimum coupling ones, dedicated SPICE simulations with extracted parasitics have been run, the results being summarized in Table 1 (C_{3D} min.).

As previously mentioned, we fit $1/C_{3D}$ with a normally distributed random variable. Hence, the probability of respecting condition (1) can be expressed as follows:

$$Y_R = 1 - \frac{1}{2} erfc\left(\frac{1/C_{3D,min} - \overline{C_{3D}^{-1}}}{\sigma_{C^{-1}}\sqrt{2}}\right); \qquad (6)$$

this relation is the probability that $1/C_{3D} \leq 1/C_{min}$; $\overline{C_{3D}^{-1}}$ and $\sigma_{C^{-1}}$ represent the mean and standard deviation of $1/C_{3D}$. The results of this approach are summarized in Table 1: large electrodes are really reliable and are only slightly affected by assembly variations; 8x8μm^2 ones show a lower parametric yield because of the small inter-electrode coupling.

7. PERFORMANCE OF CAPACITIVE INTERCONNECTIONS

The performance of AC interconnections is determined by conditions (2-3). In order to predict the parametric yield as a function of working frequency, let us perform a statistical analysis of propagation delays. $T_{3D,-} = T_{D,-} + T_{CLK,-}$ will account for data propagation and for the inter-chip clock skew during transmission as well as during preset ($T_{3D,TX} = T_{D,TX} + T_{CLK,F}$ and $T_{3D,PRE} = T_{D,TX} + T_{CLK,F}$ respectively). Variability on setup time and clock duty-cycle are not related to 3D capacitive coupling, so they are not included in our analysis. Any timing uncertainty (such as clock jitter) will be accounted for in the additional margins $T_{TX,m}$ and $T_{PRE,m}$.

7.1 Timing Analysis

In order to find out the distributions of delays along the vertical path, a statistical analysis using Monte Carlo SPICE simulations is the first step of the yield evaluation. The statistical variations are applied to the communication capacitance while the inter-channel cross-talk is taken into account by nominal coupling parameters. No statistical variations are applied to standard manufacturing parameters, such as

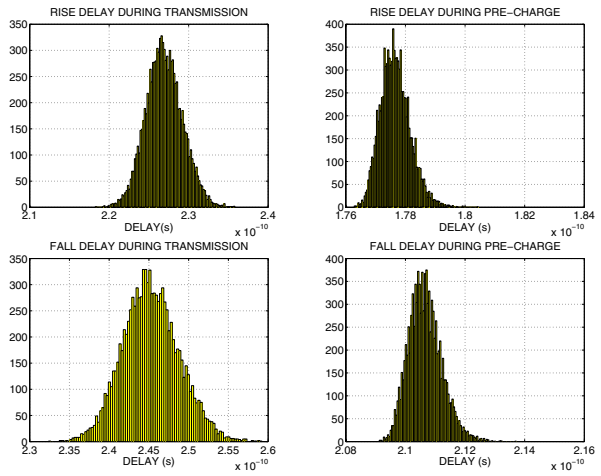

Figure 6: Delay distributions for propagation along 8x8μm^2 synchronous interconnections.

Side	$T_{TX,F}(ps)$	$T_{TX,R}(ps)$	$T_{PRE,F}(ps)$	$T_{PRE,R}(ps)$
$8\mu m$	247/3.45	228/2.5	212/0.56	178/0.49
$15\mu m$	229/1.2	242/2.4	231/0.48	198/0.61
$25\mu m$	239/3.2	267/2.5	268/2	239/1.44
Clk	$T_F(ps)$		$T_R(ps)$	
$15\mu m$	100/9.7		100/4.3	

Table 2: Mean and Standard Deviation of Delays.

gate length or wire size, since 3D technology is the only source of variation considered. Fig. 6 presents the statistical distributions of delays along an 8x8μm^2 link; they are related to transmission and to pre-charge as well, since they both determine the performance of communication. The results of Monte Carlo simulations are summarized in Table 2: the data propagation delay as well as the estimated inter-chip skew of the local clock tree are summarized as a function of electrode size.

Fig. 6 shows the quasi-Gaussian trend of propagation delays during transmission: they are almost linear as a function of $1/C_{3D}$. The pre-charge times are affected by some more non-linearities; however, this is of little concern, since the pre-charge constraints are looser than the transmission ones.

The parametric yield of the vertical interconnections can now be calculated. In order to compute the overall uncertainty along the 3D link, all logic gates that belong to the vertical path must be considered and the variability of each of them must be convoluted. In order to perform this analysis, a linear approximation is applied to relations between delay and the inverse of inter-electrode capacitance (C_{3D}^{-1}). By applying the principal component decomposition discussed in [9] and [10], the propagation delay of a logic gate can be expressed in the form:

$$d = d_0 + k_{3D} C_{3D,norm}^{-1} + \sum_i k_i p_i;$$

where d_0 is the expected value of propagation time, $C_{3D,norm}^{-1}$ is the normalized distribution of the inverse of inter-chip capacitance (normally distributed with zero mean and unit variance) and p_i are the orthogonal principal components of die parameters. Since the variability of inter-electrode coupling due to die variations is negligible compared to the impact of assembly technology, $C_{3D,norm}^{-1}$ and p_i are orthogonal.

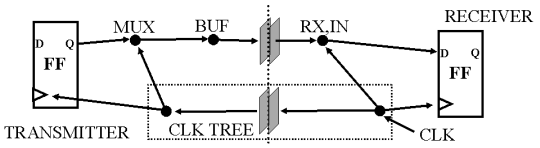

Figure 7: Block representation of the vertical path.

For application of the statistical timing analysis methodology, let us consider the signal path sketched in Fig. 7: data propagation starts on the transmitter chip; the signal propagates from the transmitter to the receiver, where it is sampled. The overall propagation time can be expressed in the form:

$$T_{3D,-} = \sum_j d_{0,j} + \left(\sum_j k_{3D,j}\right) C_{3D,norm}^{-1} + \sum_i \left(\sum_j k_{i,j}\right) p_i;$$

$$\overline{T_{3D}} = \sum_j d_{0,j}; \quad \sigma_{3D}^2 = \sum_i \left(\sum_j k_{i,j}\right)^2 + \left(\sum_j k_{3D,j}\right)^2. \tag{7}$$

where j indicates the j-th block of the path. These definitions are strictly valid under the assumption of a full correlation among the coupling variations of all vertical interconnections (for instance data and clock interconnections). This corresponds to the placement of all interconnections in a small area with respect to chip size, resulting in an equal misalignment and inter-electrode gap for all structures belonging to a stack of chips. Otherwise, $C_{3D,norm}^{-1}$ is not uniform and must be decomposed into principal components as well [9, 10].

7.2 Results

In order to predict the parametric yield, two different AC propagations are considered (according to the signal path sketched in Fig. 7): one for the clock and one for the data. The data propagation is fully embedded in the RX-TX structures and this permits a statistical analysis that is almost independent of the rest of the system. By assuming total correlation of the stacking effects and by limiting the analysis to the assembly parameters, the variances of vertical delays (precharge and transmission) can be expressed as follows:

$$k_{3D,-} = \rho_D \sigma_{DATA,-} + \rho_{CLK} \sigma_{CLK,-}; \tag{8}$$

where each ρ_D (ρ_{CLK}) is the sign of the correlation coefficient between $T_{D,-}$ ($T_{CLK,-}$) and C_{3D}^{-1}.

From the combination of conditions (2-3) and definitions (7-8) we get:

$$k_{3D,-} C_{3D,norm}^{-1} < \overline{\Delta T_-} - T_{-,m}; \tag{9}$$

In this test-case, the positive coefficient of clock propagation dominates the others, so $k_{3D,TX}$ and $k_{3D,PRE}$ are both positive and the yield can be calculated as the worst case between the conditions above. The first term of conditions (9) is a normally distributed random variable with zero mean; $k_{3D,-}$ are the cumulative standard deviations. The probability that both relations are met is given by:

$$Y_T = 1 - \frac{1}{2} erfc\left(\frac{\overline{\Delta T_{TX}} - T_{TX,m}}{k_{3D,TX}\sqrt{2}}\right); \tag{10}$$

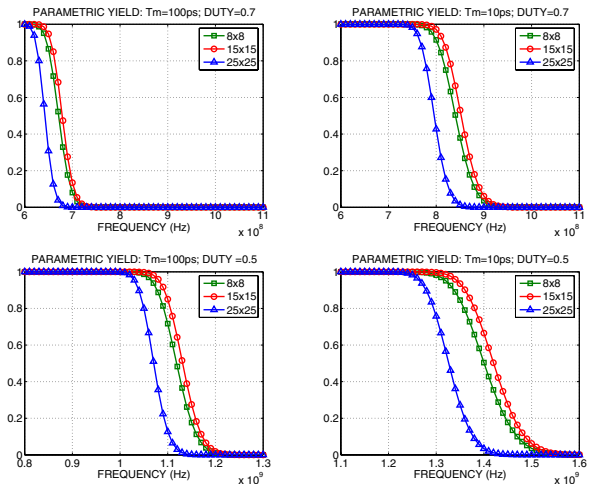

Figure 8: Parametric yield of different interconnections and different values of $T_{TX,m} = T_{PRE,m} = T_m$ and duty-cycle.

when

$$\frac{\overline{\Delta T_{PRE}} - T_{PRE,m}}{k_{3D,PRE}} > \frac{\overline{\Delta T_{TX}} - T_{TX,m}}{k_{3D,TX}};$$

otherwise, the yield will be determined by the pre-charge condition. If $k_{3D,TX}$ and $k_{3D,PRE}$ had different signs, both conditions (9) should be considered.

Results for 8x8μm^2, 15x15μm^2 and 25x25μm^2 capacitive channels are presented in Fig. 8: the results are related to different values of $T_{TX,m} = T_{PRE,m}$ and clock duty-cycle. Fig. 8 points out the relation between electrode-size and performance: in order to get maximum performance, the trade-off between large inter-electrode coupling (25x25μm^2) and small parasitics (8x8μm^2) must be exploited; so, the intermediate electrode (15x15μm^2) shows the best parametric yield, as suggested by test results in [1]. It is worth noting that the parametric yield presents a sharp decrease: it changes the order of magnitude in just a few tens of MHz. Moreover, it is important to point out how 3D independent parameters can have a strong impact on interconnection performance: for instance, if one changes the duty cycle from 0.5 to 0.7, the performance is ∼40% reduced.

8. CONCLUSIONS

A statistical analysis for 3D capacitive interconnects has been presented. Data were extracted from a sample of manufactured 3D capacitive interconnect assemblies and compared with the analytical description. Since the vertical path is fully embedded in the transmitter-receiver sub-domain of this 3D interconnect, the analysis can be confined to the vertical links. Since the assembly procedure does not affect the standard manufacturing process, the inter-electrode capacitance can be decoupled from all other sources of variation. A statistical timing analysis was applied to evaluate bit-rate constraints. Conditions for reliable interconnections were given and applied to capacitance variability.

Future work will involve reduction of extraction time (Table 3) for inter-electrode parasitics and more accurate variance estimation exploiting analytical models and optimized Monte Carlo methods.

	PHYSICAL		SPICE	
	single	cross	single	cross
8x8μm^2	13.5s	154s	8s	16.5s
15x15μm^2	66s	487s	8s	16.5s
25x25μm^2	308s	3430s	8s	16.5s

Table 3: Time-per-Iteration of MC analysis.

Acknowledgments

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