# Tutorials

**A1 Formal Verification for Real-World Designs: Today's Technologies**

Organiser: Valeria Bertacco, Michigan U, US
Speakers: Valeria Bertacco, Michigan U, US
David Cyrluk, Kestrel Inst., Palo Alto, US

This tutorial addresses state-of-the-art methods used to verify properties of sequential digital systems. The focus is on providing an overview of the main technologies and their applicability to complex designs. We cover the core algorithms involved in model checking, symbolic simulation and theorem proving methods, their application for specific aspects of formal verification and their deployment in verification software currently available both from industry and from academia.

The tutorial is intended for designers and CAD engineers interested in a better understanding of current formal verification technologies, their growth potential, and the critical CAD needs in this area.

**B1 Breaking the Synchronous Barrier for Systems-on-Chip Communication and Synchronisation**

Organiser: Luciano Lavagno, Cadence Berkeley Labs, US
Speakers: Luciano Lavagno, Cadence Berkeley Labs, US
Simon Moore, Cambridge U, UK

This tutorial focuses on non-synchronous chip-level timing techniques, which are based on handshaking rather than clock distribution networks, and thus are more robust in the presence of parametric variations, as well as generating less noise and electro-magnetic emissions. After setting the scope and related technology trends, we will cover Globally Asynchronous Locally Synchronous (GALS) design techniques. Then we will describe a novel design style that implements asynchronous circuits starting from a synchronous synthesisable model and using traditional design tools.

The tutorial is aimed at SoC architects and designers who have a background on synchronous design and want to learn how to alleviate global synchronisation problems by using a more distributed GALS-style approach.

**C1 DFT for Low Cost Testers**

Organiser: Dimitris Gizopoulos, Pireaus U, GR
Speakers: Dimitris Gizopoulos, Pireaus U, GR
Geir Eide, Teseda Corporation, US
Al Crouch, Inovys Corporation, US
Ken Posse, Teseda Coporation, US

This tutorial focuses on how DFT can be used to enable usage of the new breed of low-cost structural test equipment. Just as DFT is more than inserting scan chains, low cost test is more than a cheap tester. With a practical approach and industry examples, this tutorial explains the characteristics and limitations of low-cost structural test equipment and methodologies, and elaborates on how the low cost structural tester fits in the design and test flow. Common DFT techniques and issues such as DC scan, AC scan, ATPG, BIST, SoC Assembly and IP reuse are explained in context of low cost test.

Intended Audience: IC/IP/SoC Design Engineers, DFT Engineers, Test Engineers, and Managers with some basic DFT knowledge, who want to learn about how DFT can be used to enable low cost test, and what low cost testers are all about.

This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program — TTEP 2004.

**D1 DfY/DfM – Design for Yield and Manufacturability (Industrial Tutorial)**

Organiser: Andreas Ripp, MunEDA GmbH, DE
Speakers: Ralf Sommer, Infineon Technologies AG, DE
Eckhard Hennig, Infineon Technologies AG, DE
Michael Pronath, MunEDA GmbH, DE
Andreas Ripp, MunEDA GmbH, DE

The tutorial presents an introduction into "DfY/DfM - Design for Yield and Manufacturability" covering basics of analogue circuit simulation, statistical analysis and design centering from both methodology/implementation as well as from the industrial application side. The tutorial presents the following six topics: introduction into DfY/DfM, basics of analogue circuit simulation, methodology for statistical circuit analysis and yield optimisation, software solutions and design flow integration, design flow specific industrial applications and use cases closing with an outlook on actual and future challenges in the DfY/DfM area regarding a global design environment.

Intended audience: analogue- and mixed-signal circuit designers, CAD- and design-support engineers (library management, technology migration and design reuse, process characterisation)

**E1 Structured CAD: Technology Closure for Modern ASICs**

Organiser: Leon Stok, IBM T J Watson Research Center, US
Speakers: Leon Stok, IBM T J Watson Research Center, US
Juergen Koehl, IBM Microelectronics, Boeblingen, DE

Much attention has recently been paid to structured ASICs: they potentially lower manufacturing cost and alleviate certain design problems by providing predefined gates, power grids, clocks and test. Unfortunately, this comes at a significant expense in silicon efficiency being it power, delay or area. A structured CAD methodology, with appropriate algorithms and tools, combined with a solid technology library and chip footprint, will give predictable chip design turn-around times and first-time right silicon, without the loss of silicon efficiency. This tutorial will describe a structured CAD methodology and tools to design high-end ASICs. Design examples from IBM's ASIC methodology will show the applicability of these algorithms to designs with three million plus placeable objects at Ghz speeds.

Intended audience: This tutorial is intended for designers to get an insight in RTL-to- layout design methodologies, and find out what works and what does not, for CAD-tool developers to understand state-of-the art algorithms for rapid design closure on large designs and for their managers to get an insight in the applicability of these techniques to their specific design problems.

**F1 Programming Models for Multiprocessor SoC (full-day)**

Organiser: Ahmed Jerraya, TIMA Laboratory, FR
Speakers: Frank Pospiech, TIMA Laboratory, FR
Ahmed Jerraya, TIMA Laboratory, FR
Rolf Ernst, TU Braunschweig, DE
Giuseppe Desoli, STMicroelectronics, CH

A programming model provides an abstraction for HW-SW Interfaces and allows concurrent design of complex systems made of sophisticated software and hardware platforms. Examples include API at different abstraction levels, RTOS libraries, drivers, typically summarised as Hardware dependent Software (HdS). This abstraction smoothes the design flow and eases interaction between different teams belonging to different cultures, hardware, software and system architecture. This Tutorial deals with the application of this concept to MPSoC and:

1. Introduces the concept of Hardware dependent Software (HdS) for MPSoCs and discusses the status of related standardisation efforts. HdS is aimed to de-couple HW and SW designs and handles efficiently complex issues like distributed boot, bring-up, and communication inside and outside an MPSoC.
2. Explores HW-SW Interfaces abstraction for heterogeneous MPSoC based on complex communication protocols and topologies. Different abstraction schemes and Transaction-Level-Modelling (TLM) will be explored to ease different design steps including SW and HW design, integration, debug and validation.

3. Addresses modelling for analysis and optimisation of MPSoC architectures including hardware and software layers such as drivers, run-time systems and application APIs. Different scheduling strategies, communication behaviours and performance requirements must be matched and combined on a single system.
4. Presents the DELI experience to show that application level software development can be overlapped with the development of the rest of the system. DELI is aimed to generating portable HdS taking into account real-time constraints and low-level interactions with OS and the HW during early prototyping.

**A2 The Coming of Age of Reconfigurable Computing - Potentials and Challenges of a New Technology**

Organiser: Walid Najjar, UC Riverside, US
Speakers: Walid Najjar, UC Riverside, US
Fadi Kurdahi, UC Irvine, US
Kees Vissers, UC Berkeley and Xilinx, US

Platforms that combine CPUs with a reconfigurable fabric on the same chip have been recently introduced. Such devices are ideally suited for many application domains ranging from multimedia to communication. A major challenge to their wider use is the lack of high level programming and design space exploration tools. This tutorial focuses on three aspects of this emerging technology: (1) the intrinsic potential of the temporal/spatial paradigm (2) The wide range of architectures, fine and coarse grained, and the trade-offs between performance and flexibility. (3) A survey of current and future applications in multimedia and mobile communication and analysis of their performance and energy requirements. It is intended for an audience of developers and researchers in high-end embedded systems.

**B2 Reliable Design: A System Perspective**

Organiser: Giovanni De Micheli, Stanford U, US
Speakers: Giovanni De Micheli, Stanford U, US
Ravi Iyer, Illinois U, Urbana Champaign, US

The tutorial presents methods for reliable system design. We consider systems realised on a single chip, systems consisting of several integrated components (possibly components off-the shelf - COTS), and distributed systems. We address both hardware (computation and communication) and software aspects of reliable system design.

This tutorial is intended for researchers in EDA, system/chip designers and software developers for integrated systems, as well as for managers who want to learn about reliable design and how this area evolved in view of the current technology trends.

**C2 Defect Diagnosis and Silicon Debug: The Continuing Detective Story**

Organiser: Dimitris Gizopoulos, Piraeus U, US
Speakers: Srikanth Venkataraman, Intel Corporation, US
Rob Aitken, Artisan Components, US

The tutorial covers a spectrum of diagnosis and debug topics from the basic concepts to future challenges, over the life-cycle of a product. Established diagnosis procedures fault dictionaries, post-test fault simulation, and hardware-based backtracking will be discussed, followed by recent enhancements and advanced diagnosis topics, including methods for locating defects, approximation techniques for identifying unmodelled faults, deductive analysis, Iddq-based diagnosis, diagnosis for delay-faults, scan-chain diagnosis, BIST-based diagnosis, and design-for-diagnosability techniques. The tutorial then will focus on silicon debug techniques, design-for-debug techniques, and applications to yield improvement. Successful diagnosis methods used in real industrial products, industrial experiences, and case studies will be presented in this tutorial.

Intended Audience: Design, validation, test and failure analysis engineers, researchers, managers, and anyone else determined to find out where those puzzling errors are coming from.

This tutorial is part of the IEEE Computer Society TTTC Test Technology Educational Program — TTEP 2004.

**D2 Stuctured ASIC Tutorial: Essential Information on Devices and Design Flow (Industrial Tutorial)**

Organisers/: Christoph Hecker, NEC Electronics Europe, DE
Speakers: Doug Amos, Synplicity, Europe, UK

ISSP (Instant Solution Silicon Platform), the leading Structured ASIC Technology, was of great interest when introduced by NEC Electronics at DATE 2003. Now this tutorial will give you all the essential information required to judge the competitive advantage that using Structured ASIC can give you in your next project.

ISSP devices are mask-programmed to your specification with very low NRE costs and short lead time. The Design is implemented through the optimised and dedicated synthesis technology of Synplicity's Synplify ASIC tool.

This tutorial shows how you can use either your ASIC or FPGA expertise to use ISSP without excessive tool costs or massive re-training.

**E2 Advanced Domino Circuit Design**

Organiser: David Harris, Harvey Mudd College, US
Speakers: David Harris, Harvey Mudd College, US
Tom Grutkowski, Intel Corporation, US

Despite rumours of their demise, domino circuits are still indispensable in the design of high speed CMOS chips because they offer a 1.5-2x performance advantage over static logic. This tutorial briefly reviews basic dominio design issues, then compares and contrasts a wide variety of high-performance domino and nonmonotonic dynamic sequencing techniques. It then details the domino methodology used on the Itanium 2 microprocessors and explores pitfalls discovered during silicon debug.

This tutorial is intended for circuit, logic, CAD, and test engineers interested in high-performance domino design.