Should Our Power Approach Be Current?

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Abstract
In the past, power consumption was of little concern to the IC designer. Time-to-market drove the design deadlines, and power consumption was a secondary, if not tertiary, concern. If there were power issues, they could typically be accounted for by tweaking the fabrication process, redesigning after the initial design ship, or even just waiting for the next process change from the fab.

Today power has become one of the sign-off qualifiers prior to fabrication, and the metric for success has changed from performance and area to power consumption in nanometer SoC designs, especially in the huge market for handheld/wireless consumer electronics. Although "power" is often the stated concern, current is the real issue. This fundamental paradigm shift requires changes to both the design flow and the tools used for electrical sign-off.

Categories and Subject Descriptors
B.7 Integrated Circuits

Keywords
Low-power design, power analysis, leakage current, energy consumption, static power, dynamic power

The Challenge below 90-nm
At 65nm and below, leakage current can dominate the active power consumptions and become a key issue for virtually all designs. Subthreshold and gate leakage components caused by lower threshold voltages, thinner oxides, and shorter channel lengths can result in smaller noise margins and increasing chip failures.

To properly address the problem of power consumption (either static or dynamic), the solution must be both *accurate* and *fast*. A fundamental shift, from voltage-based applications to current-based applications, needs to be undertaken so as to best address both of these needs simultaneously while still fitting within the current IC design flow.

Tim Fox, a senior analyst for Deutsche Bank Equity Research, will moderate a series of questions for the panelists, represented by leading semiconductor vendors and tool providers, to discuss the approaches they are taking and debate the ownership and requirements for solving the complex issue of leakage current management

Questions such as:

> Has the low power problem been solved for 90-nm and is the focus now on 65-nm?
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> Is this primarily a problem for the process engineer or the circuit engineer or both?
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> What capabilities do process or design engineers need to address the issue of leakage? How many of those capabilities are available today?
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> What solutions can EDA vendors provide to help manage leakage current?
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> Will we ever be able to make leakage a minimal concern for future process nodes?

DAC 2005, June 13–17, 2005, Anaheim, California, USA.
ACM 1-59593-058-2/05/0006.