

Circuit Design of a Wide Tuning Range CMOS VCO with Automatic Amplitude Control

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ABSTRACT

A novel tuning mechanism to greatly widen the frequency tuning range of VCO is presented. A tuning range of over 50% has been achieved for a CMOS VCO with the adoption of this technique. Moreover, a constant amplitude control loop is also incorporated in this circuit, ensuring stable oscillation amplitude over the whole tuning range.

Categories and Subject Descriptors

B.7.1 [Integrated Circuits]: Types and Design Styles – VLSI (very large scale integration).

General Terms

Design

Keywords VCO, CMOS, tuning range, automatic amplitude control.

1. INTRODUCTION

As a very important block for RF transceiver system, voltage controlled oscillator impacts many performances of the whole system. With the ceaseless advance of CMOS technology, it is becoming more and more attractive for the integration and implementation of such a system.

The traditional LC oscillator can be modeled with a RLC parallel network, in which a variable capacitor is used for frequency tuning [1]. But due to the absence of good varactor compatible with CMOS process, the tuning range of integrated CMOS LC-type VCO is typically lower than 20% of the centre frequency [2, 3, 4].

Since the lot-to-lot process variations in on-chip capacitance and inductance may be as large as 20%, the oscillation frequency may also have an error of 20% or more for lot-to-lot difference. The tuning range of VCO must be wide enough to compensate for the fluctuation.

A CMOS ring oscillator with 50% tuning range has been demonstrated in Ref. [5]. A LC oscillator which is tunable from 1.34GHz to 2.14GHz is reported in Ref. [6], by connecting two inductors in parallel, and changing the inductance by switching one of them from cut-off to turn-on. It needs more area-hungry inductors, and the tuning range is limited by the ratio of the two inductors in parallel.

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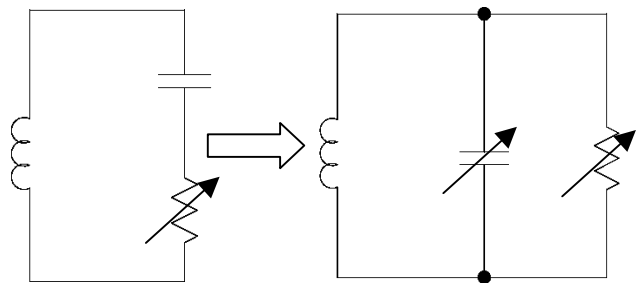
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Here a novel tuning mechanism to broaden the frequency tuning range of LC VCO is proposed. By tuning the resistance in series with a capacitor, a tuning range of over 50% has been achieved for a CMOS VCO with the adoption of this technique. Moreover, a constant amplitude control loop is also incorporated in this circuit, ensuring stable oscillation amplitude over the whole tuning range.

2. TUNING PRINCIPLE

As shown in Figure 1, the circuit in (a) containing serially connected resistor R_S and capacitor C_S can be transformed to its parallel form, showing in (b) of this figure.



Equating the real parts and imaginary parts of the impedances of the series and parallel RC sections respectively, the following transformation formulas can be achieved:

$$C_P = \frac{C_S}{1 + \omega^2 C_S^2 R_S^2} \quad (1)$$

$$R_P = R_S + \frac{1}{\omega^2 C_S^2 R_S} \quad (2)$$

It can be seen from equation (1) that C_P is variable if R_S is a tunable resistor controlled by a voltage. The oscillation frequency of this LC is given by:

$$f_0 = \frac{1}{2\pi \sqrt{LC_P}} \quad (3)$$

By tuning the resistance of R_S , the equivalent parallel capacitance C_P is changed, and then the oscillation frequency is changed also. This is the tuning principle of this circuit.

The tunable resistor R_S can be realized through a MOSFET with its gate connected to a control voltage, which can be implemented very easily with CMOS technology. The capacitor C_S can be realized with MIM (metal-insulator-metal) capacitor, which is also a standard process in mixed-signal CMOS process. Thus this novel approach eliminates the need of varactors.

It can be seen from equation (1) that when R_S approaches zero, C_P will be close to C_S , and when R_S approaches infinite, C_P will be close zero. So theoretically, the frequency tuning range can be:

$$\left(\frac{1}{2\pi\sqrt{LC_S}}, \infty \right) \quad (4)$$

For on-chip MIM capacitor, there is a parasitic capacitor between the lower plate of it and the substrate. The value of this parasitic capacitor can be one tenth or more of the nominal value of the MIM capacitor generally, and it determines a rough upper limit of the frequency range. If we nominate this capacitance as C_{ox} , the frequency tuning range can be revised as

$$\left(\frac{1}{2\pi\sqrt{LC_S}}, \frac{1}{2\pi\sqrt{LC_{ox}}} \right) \quad (5)$$

In above equation, the ratio of the upper limit to the lower limit is about three.

But in reality, the tune-on resistance of a MOSFET can not be zero, and there exists parasitic capacitance of on-chip MOSFET-type resistor. MIM capacitor and other devices connected to this point will set an upper limit to the oscillation frequency much lower than infinite.

3. PROPOSED CIRCUIT ANALYSIS

The differential VCO is shown in Figure 2. The on-chip spiral inductor L and MIM capacitor C forms the resonant tank, and MOSFET M0 is controlled by the tuning voltage as the variable resistor. The cross coupled differential pair formed by M1 and M2 is used to keep the oscillation.

The frequency sensitivity is an important parameter of VCO, determining by the characteristic of M0. The turn-on resistance of M0 may change sharply when the control voltage is near its threshold voltage, and a small variation of the control voltage may cause a large fluctuation of oscillation frequency. To alleviate this problem, several types of MOS transistors with different threshold voltages are connected in parallel.

As shown in equation (2), the equivalent parallel resistance R_P will decrease to a minimum value then increase when M0 changes from cut-off to fully turn-on. This minimum value is given by:

$$\min R_P = \frac{2}{\omega C_S} \quad (6)$$

At this time, the network is lossiest. So the bias point and size of M1 and M2 must be determined to have a minimum acceptable transconductance for guaranteeing oscillation. This is expressed as:

$$\min g_m = \frac{1}{\min R_P} = \frac{\omega C_S}{2} \quad (7)$$

Since the equivalent parallel resistance R_P may vary vastly during the whole tuning range, the oscillation amplitude can also be very different. Too large oscillation amplitude may destroy the gate of MOSFET, and this problem is more and more serious as the gate oxide becomes thinner and thinner with improve of CMOS technology. Not only that, too large oscillation amplitude can also degrade the phase noise performance [4]. Furthermore, stable oscillation amplitude over the whole frequency tuning range is desirable for mixers. These make the amplitude regulation necessary [5-6].

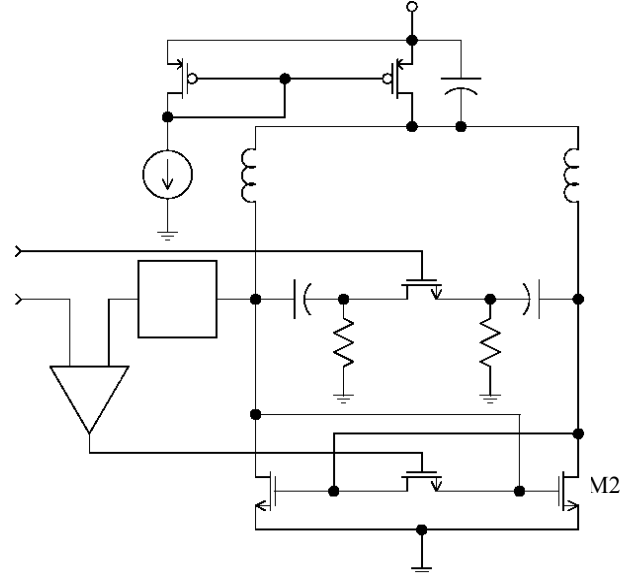


Figure 2. Schematic of the proposed VCO

Figure 3 shows the schematic detail of the peak detector. It output is controlled by two currents: push and pull. When the input terminal is larger than the output, a large current is injected to the output terminal, making its voltage rise fast; when the input terminal is smaller than the output, a small current is drained from the output terminal, making its voltage decrease slowly. Thus the output can track the peak value of the input oscillation. The values of the push current and pull current decide the attack time and the decay time of this circuit, which should be determined by applications.

The schematic detail of the OTA is shown in Figure 4. Its pull current I_{PULL} is a constant current, while its push current I_{PUSH} is decided by the difference of the input terminal voltage and the reference voltage V_{REF} . When V_{IN} equals V_{REF} , then I_{PUSH} equals I_{PULL} , and the voltage of the output terminal keeps stable. The NMOS transistor MC is connected as a capacitor, saving silicon area and achieving faster charge time due to its low capacitance when V_{OUT} is smaller than its threshold voltage, compared with traditional MIM capacitor.

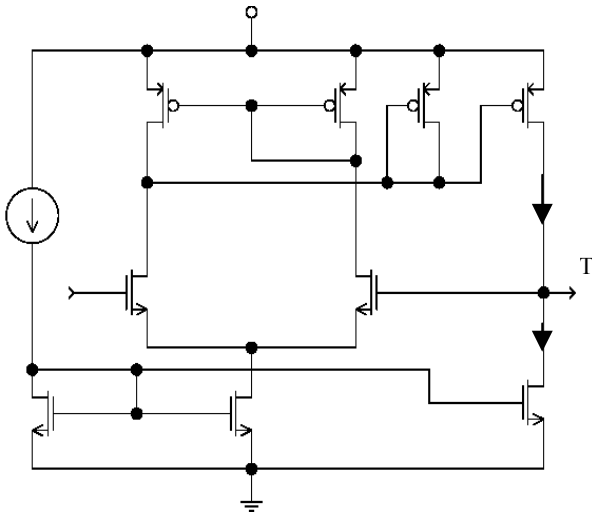


Figure 3. Schematic of the peak detector

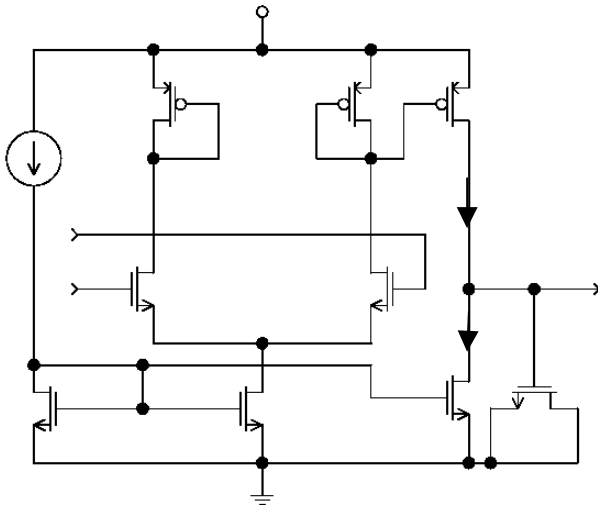


Figure 4: Schematic of the OTA

4. SIMULATION RESULTS

This circuit is designed and simulated by using 0.18 μm mixed-signal CMOS process with 1.8-V supply voltage to the correctness of the design. All devices are real with their parasitic provided by the foundry, including MOS transistors, MIM capacitors, on-chip spiral inductors, and resistors. No idealized components are included, such as the current sources shown in above circuits.

Figure 5 shows the tuning characteristic of this circuit. The minimum oscillation frequency is 1.75GHz, while the maximum oscillation frequency is 3.16GHz, achieving a tuning range of 57%, much wider than the works previously published.

The amplitude regulation function is also verified. The reference voltage is set to make the peak-to-peak value of the oscillation amplitude stabilized at about 0.6V. Figure 6 shows the stabilization process of the oscillation amplitude when the tuning

voltage is set to zero. It can be seen that the initial amplitude reaches near 4V, which is close to the gate break-down voltage. After about 800 ns, the amplitude is stabilized and regulated to about 0.6V.

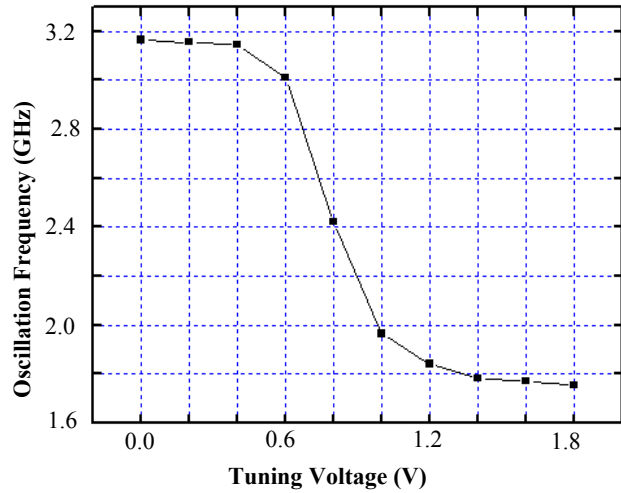


Figure 5. Simulated oscillator tuning characteristic

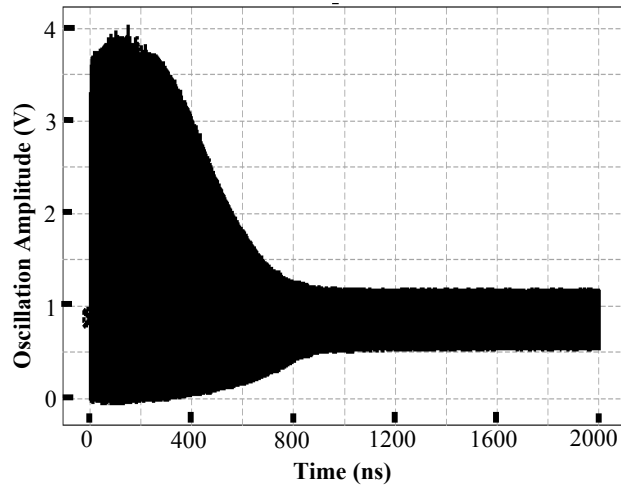


Figure 6. Stabilization process of the oscillation amplitude

The oscillation amplitude as a function of tuning voltage is also studied with the results shown in Figure 7. It can be seen that without automatic amplitude control, the amplitude variation exceeds 2.8V over the whole tuning range, and the maximum amplitude reaches about 4V, exceeding twice of the power supply voltage. While with the automatic amplitude control, the amplitude variation is about 0.15V over the whole tuning range, and the amplitude is stabilized to about 0.6V.

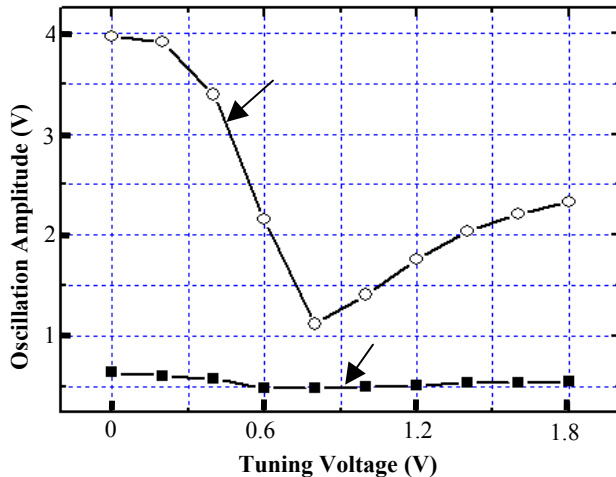


Figure 7. Comparison of the oscillation amplitude without and with automatic amplitude control

5. CONCLUSION

This paper discusses the circuit design of a wide tuning range CMOS VCO with automatic amplitude control by using the mixed-signal CMOS technology. By tuning the resistance in series with a capacitor, a tuning range of over 50% has been achieved for a CMOS VCO. To ensure stable oscillation amplitude over the whole tuning range, a constant amplitude control loop is also incorporated in this circuit. The novel tuning principle is explained, and then the implementation details and design considerations of this circuit follows. After all, the simulation results are proposed with all real devices models provided by the foundry including their parasitic, showing the correctness of our design.

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