Design Techniques for Low Power High Bandwidth Upconversion in CMOS

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ABSTRACT

An upconvertor topology for low power, high bandwidth applications is presented. Using specific circuit techniques and local circuit-level optimization, the power consumption of the total system comprising an on-chip LC-type VCO, a polyphase network quadrature generator, a linear mixer block and an RF-current buffer, has been minimized.

A chip has been designed and manufactured in a 0.25μm CMOS technology. The VCO oscillates between 1.68 GHz and 2 GHz. Driven by an external LO, the transmitter operates from 900 MHz up to 2 GHz. At 2 GHz, the upconvertor transmits -12 dBm into 50 Ω with a linearity of more than -35 dBc for base band signals up to 33 MHz.

Categories and Subject Descriptors

B.7.m [**Integrated Circuits**]: Miscellaneous—*Analog RF CMOS Design*

General Terms

Design

Keywords

Low power, Analog, Upconversion, Oscillators, RF Design, CMOS

1. INTRODUCTION

1.1 Wireless Systems

In the post-GSM era a few new communication standards for mobile and portable devices are waiting for being introduced into the business and consumer markets. The recently adopted UMTS-standard, operating in the 2 GHz range is such a candidate to be selected for the implementation of new *mobile* services on devices like PDA's or cell phones. This standard implements data rates for mobile terminals up to 384 kbps over a bandwidth of 5 MHz using CDMA [1].

For *portable* devices as laptops, generally higher data transmission rates are required. Standards as IEEE 802.15.3 are being developed, providing a data rate of 55 Mbps over a bandwidth of 15 MHz using 64 QAM modulation with Trellis coding [2]. This speed of wireless transmission is also envisaged by the Hiperlan/2 [3] standard that 0 data rates up to 54 Mbps over a channel 16.25 MHz wide. Here OFDM is implemented using 52 subchannels of which 48 are used as data channels. According to [2], a SNR of more than 20 dB is needed in the receiver to operate at a BER of 10^{-5} or better when receiving a 64 QAM+TCM-modulated signal. The transmitter will need an SNR that is even higher to ensure proper system operation. The UMTS standard mentioned in the previous paragraph also defines an indoor wireless transmission speed up to 2 Mbps for non-moving (portable) devices, using the same bandwidth of 5 MHz.

As a comparison: the channel bandwidth of a GSM system is 200 kHz, the needed SNR is about 9 dB ([4]). Conclusion of this very brief overview is that in the chip-sets that are to provide high data rates, a signal with a high SNR and a bandwidth some order of magnitudes larger than for first-generation mobile terminals, must be dealt with.

1.2 Previous art

A lot of effort has been spent in the design in CMOS of complete transceiver systems for low data rate, i.e. small band, mobile systems. This resulted in some successful designs in both research and commercial environments [5, 6, 7]. Recent research has shown the possible use of a CMOS upconvertor that combines low power consumption with sufficient power output at frequencies up to 2.4 GHz in a system with data rates already an order of magnitude higher than those of first and second generation wireless devices [8].

1.3 This paper

In this paper, some circuit techniques are presented that have been used in an upconvertor implemented in a 0.25μm CMOS technology. The focus lies on techniques that enable the transmission of a base band signal with a large band-

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width and high SNR, without creating a large increase in power consumption.

In a first section, a design overview deals with the global topology of the upconvertor, the used design methodology and the RF-MOST model used for circuit simulations. Then, the building blocks are reported in detail, starting with the LC-oscillator. The following section handles the polyphase network. Section 5 and Section 6 deal with the implementation of the linear mixer block and of the output buffer, respectively. Section 7 discusses the measurements. After that, the conclusions are formulated.

2. DESIGN OVERVIEW

2.1 Global Topology

Fig. 1 shows the block schematic of the implemented upconvertor topology.

The first block is an LC-type VCO, that delivers a differential signal to the polyphase network. By this network it is converted into a quadrature LO signal. The input of the polyphase network is coupled capacitively to the oscillator and the output is directly connected to the quadrature mixer block. The base band input of the mixer block is a differential quadrature signal, applied externally. A high pass network acts as an RF/LF splitter at the output of the mixer block to short all low frequency components to ground while passing all RF signals to the RF current amplifier. A 50 Ω output match is implemented as a series inductor and parallel capacitor using on-chip components.

2.2 Design Methodology

The design methodology used is aimed at a minimization of the total power consumption and consists of a global design on block-specification level and a local optimization on circuit level for each functional block or set of functional blocks. Together with the indication of the specific circuit techniques used, this local optimization will be discussed for each part separately.

2.3 RF-MOST modelling

At the start of the design, no RF-models for the MOS-transistors were available. Therefore, a transistor subcircuit has been constructed using the following approach ([9]):

- From the available BSIM3-models an *intrinsic* MOST model is derived by setting all junction-areas to zero;
- The junctions are added as diodes in the RF-MOST subcircuit, resulting in higher accuracy of the junction capacitor values for low finger numbers;
- Source, drain and substrate resistors are added to the subcircuit;
- A layout-related coupling capacitor between source and drain is added;
- A physical gate resistance is added.

In simulations, the non-quasi-static effect has been found to be negligible for the building blocks and frequencies used in this design. Therefore, it is not added to the RF-MOST subcircuit.

3. LC-TYPE VCO

3.1 Topology and Design

The implemented topology for the VCO is shown in Fig. 2.

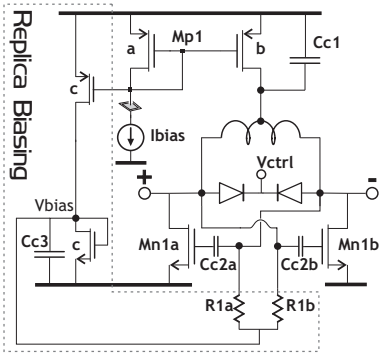

Figure 2: VCO topology with capacitively coupled gain cell transistors

The LC-tank of the oscillator is constructed using an on-chip symmetrical coil and PN-junction diodes of which the capacitance value is controlled by voltage V_{Ctrl}. The inductor has a central tap to which the pMOST bias current source $Mp1b$ is connected. The 1/f noise of this current source is reduced by setting the channel length to 2μm instead of the minimal 0.25μm. To further restrain 1/f-noise of this transistor from entering the circuit, the central tap is decoupled by the large on-chip capacitor $Cc1$.

The gain cell consists of nMOST pair $Mn1$, of which the gates are coupled to the LC-tank by capacitors $Cc2$. These capacitors effectively decouple the DC output level of the oscillator from the DC biasing voltage of the gain cell. Here, the gain cell biasing is done by a replica biasing of the pMOST current source $Mp1a$ connected in series with nMOST diode $Mn1c$ having the same aspect ratio as the gain cell transistors. The gate of each gain cell transistor $Mn1$ is connected to the resulting replica bias voltage using a large resistor ($R1$) as depicted in Fig. 2. Capacitor $Cc3$ is a low impedance to ground for the noise current of the two resistors.

3.2 Optimization

The optimization of the VCO consists of two parts. First, global optimization of the VCO has been done using an in-house tool [10]. Secondly, an optimal value for resistors $R1$ and capacitor $Cc3$ of Fig. 2 has been determined, minimizing the influence on the phase noise of the VCO. This optimization has been performed based on circuit simulations using a proprietary phase noise simulator [11].

Since the DC level at the output of the oscillator can be chosen freely, an optimal value is applied that maximizes the output voltage swing. The result is that no buffers are needed after the VCO to drive the polyphase network. Since the role of these buffers is to provide a low output impedance at RF frequencies, a considerable amount of power can now be saved. Moreover, setting the DC voltage to this optimal value simultaneously maximizes the symmetry of the oscillator signal. According to [12] this ensures a low upconversion of common-mode 1/f noise (e.g. the 1/f noise current from $Mp1b$).

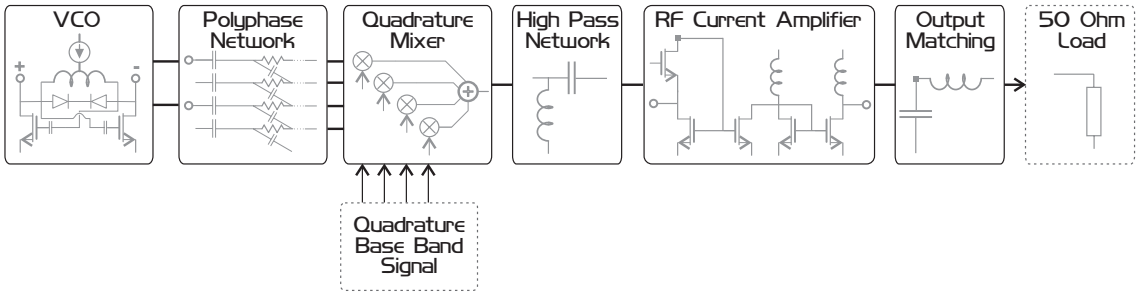

Figure 1: Global upconvertor topology

4. POLYPHASE NETWORK

A four stage polyphase network is used to generate a quadrature LO signal for a broad range of input frequencies. In one version of the test chip, the polyphase network is driven by an external differential LO to have a larger frequency range for testing. For this block the power consumption is lowered as compared with a traditional topology by omitting the output buffers of the polyphase network and directly coupling the polyphase network to the gates of the mixer transistors.

This direct coupling demands an optimization over three building blocks. The *coupling capacitor* between VCO and polyphase network, the *total network resistance* and the *size of the mixer transistors* all influence at the same time the output current of the mixer block. The goal of the optimization is to maximize this output current, while minimizing the influence of the coupling on the phase noise of the VCO.

The influence of the circuit elements specified above are as follows:

- the polyphase network has a loading effect on the VCO, lowering its oscillation amplitude and deteriorating the phase noise;
- the polyphase network is loaded by the input capacitance of the mixer block, lowering the output amplitude of the polyphase network;
- the amplitude at the output of the polyphase network directly influences the output current of the mixer block;
- also the size of the mixer transistors directly influences the output current.

It is clear that the entanglement as described above necessitates a local optimization over a set of functional blocks, being VCO, polyphase network and mixer block.

Fig. 3 shows the Image Ratio (IR) of the output signal of the implemented polyphase network, with and without simulated worst-case mismatch effects for a yield of 99.9%.

5. LINEAR MIXER BLOCK

The used quadrature linear mixer topology, including the high pass network at its output, is depicted in Fig. 4.

To obtain a good performance of a linear mixer block, the following requirements must be fulfilled [13]:

- *to avoid LO upconversion:* a zero DC voltage drop between source and drain of the mixer transistors;

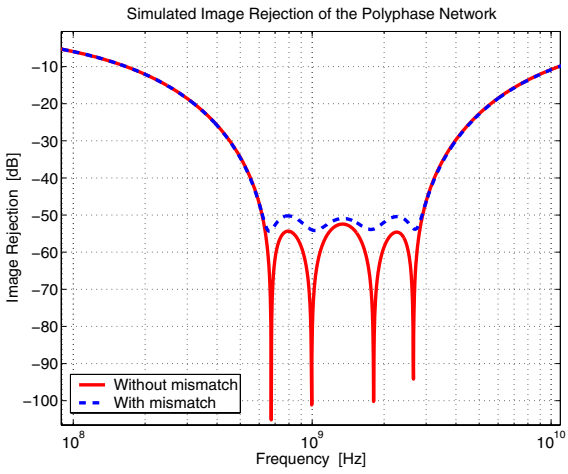

Figure 3: Simulated IR of the generated quadrature signal

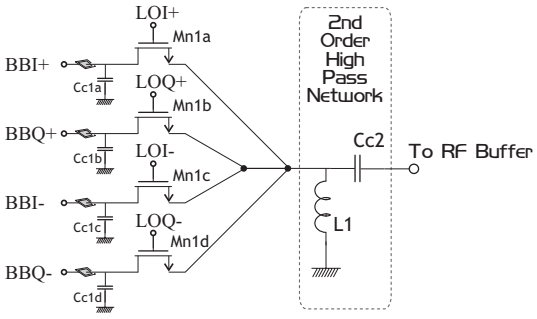

Figure 4: Mixer topology with high pass network

- *to avoid upconversion of the base band frequency f_{BB} to $f_{LO} \pm 2.f_{BB}$:* at the drain/source, a low impedance to ground for DC up to $2.f_{BBmax}$, with f_{BBmax} the maximal base band frequency;
- *to avoid degeneration of the RF output:* a low impedance for RF signals at the mixers' output and at the mixers' input.

These requirements have been implemented as follows:

- the zero DC voltage drop is realized by simply applying a baseband input signal with a zero DC value. (The mixer output is also at DC ground due to the inductor of the high pass network.);

- the high pass network realizes a low impedance to ground for low frequencies and a low impedance to the input of the current buffer for high frequencies;
- the input stage of the current buffer realizes a low impedance for RF signals at the mixers' output;
- the on-chip capacitors $Cc1$ in Fig. 4 realize a low impedance to ground for RF signals at the mixers' input.

In this building block, optimization is necessary for the on-chip inductor and the coupling capacitor of the high pass network. This optimization is to ensure that the second requirement given above is met and also that low frequencies are restrained from entering the RF current buffer.

A power efficient implementation is realized by choosing a *passive* network to discriminate between high and low frequencies. An alternative would be to use an active second order filter. Since the pass-band starts around 900 MHz and goes up to 2 GHz, this solution would consume an amount of power that is comparable to the power usage of the input stage of the RF current buffer. Moreover, the passive solution allows a further enlargement of the transmission bandwidth without power penalty by implementing a higher order passive network, albeit at the cost of a larger area consumption.

6. TWO-STAGE CURRENT BUFFER

6.1 Topology

The demands for the current buffer are twofold:

- a low input impedance for high frequencies to ensure a proper mixer operation;
- a power-efficient current amplification with sufficient output power.

The used buffer topology is depicted in Fig. 5.

The input buffer has an input admittance of gm_{Mn1} at frequencies above the GBW of the feedback loop, and of $gm_{Mn1}.G$ for frequencies below the bandwidth of the loop, with G the DC gain of the feedback loop [13]. Since the GBW of the loop is certainly lower than 2 GHz, the only way to obtain a low input impedance is by ensuring a high value for gm_{Mn1}. This is accomplished by sending sufficient current through the input stage of the buffer.

The amplification stages of the current buffer are current mirrors with a ratio $M > 1$. In the first stage, a ratio of 2 is used, and in the second stage a ratio of 3. The first stage is coupled capacitively to the second stage. Thus, pMOST bias current source $Mp2a$ only has to be sized to supply the bias current for $Mn3a$, lowering the parasitic capacitance of $Mp2a$. The (large) mirror current of $Mn2b$ is flowing through an on-chip inductive load connected to Vdd_{low}. The voltage of Vdd_{low} can be made lower than Vdd_{buffer}, because only a single transistor has to be set into saturation.

The power usage of this block is minimized by optimization of the load inductance and couple capacitance to obtain a maximum current transfer efficiency of one stage to another.

6.2 Inductor Optimization

The inductors used as load for the mirror transistors $Mn2b$ and $Mn3b$ in Fig. 5 are optimized to obtain maximum current efficiency, in other words, minimum current loss. Therefore, they are designed towards maximum parallel resistance Rp for an inductance value Ls that maximizes the 3 dB bandwidth of the buffer. The optimal inductor, having maximum Rp for this value of Ls, is found using a variant of a tool for VCO optimization [10]. This tool uses the inductor extraction program FastHenry ([14]) to calculate the values of the inductance Ls and the series resistance Rs of a coil with a given geometry. An optimization algorithm (ASA [15]) is used to find the optimal coil geometry by minimization of a cost function. In this case, the cost function CF is constructed as follows:

- $Q_{coil} = 2\pi f_0 Ls/Rs$
- $Rp = Rs(1 + Q_{coil}^2)$
- $Cost_{Ls} = |Ls_{wanted} - Ls|/Ls_{wanted}$
- $CF = w_1 \cdot Cost_{Ls} + w_2 \cdot (Rp^{-1})$

Here, f_0 is the maximum frequency of interest, Q_{coil} is the quality factor of the inductor and Ls_{wanted} is the target value for the inductance. Weight factor w_1 is set to a low value if $Ls \approx Ls_{wanted}$ and to a high value otherwise, while w_2 has a constant medium value. By minimization of this cost function, an inductor geometry is found that has an inductance value "close to" Ls_{wanted} and a maximum value for Rp. In fact, by choosing the weight-values appropriately, the optimizer is allowed to make a trade-off between a value for Ls differing slightly from the target and a higher value for Rp.

7. CHIP PHOTO & MEASUREMENTS

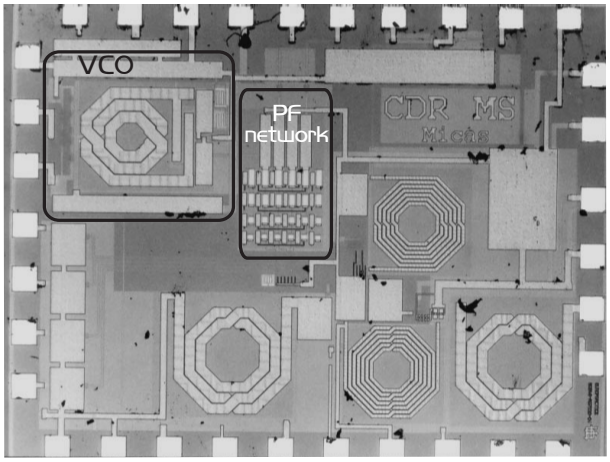

Figure 6: Chip photograph

A photo of the chip, processed in a 0.25μm technology, is given in Fig. 6. The used technology provides MMC (metal-metal) capacitors and has a substrate resistivity of 15 Ω.cm. The VCO is situated in the top left corner. Right from it, the four stage polyphase network can be seen. The two coils with small width and five turns are the two load inductors with high Rp from the current buffer. The two other coils are

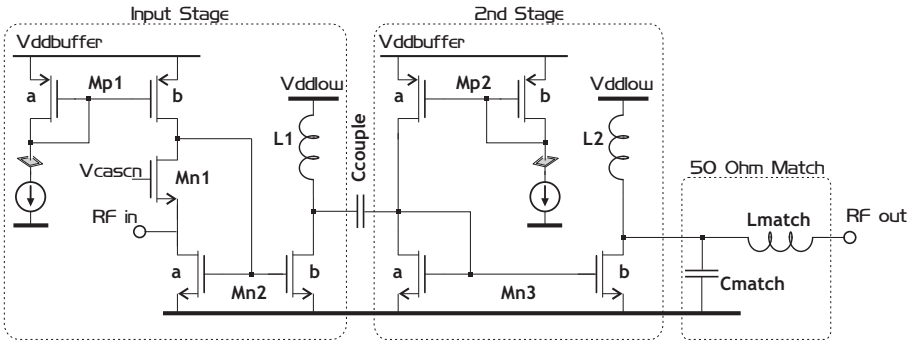

Figure 5: Two-stage RF buffer with low impedance input stage

the inductor of the high pass network and of the matching network. The chip measures 1.8x2.3 mm^2

Fig. 7 shows the tuning characteristic of the on-chip VCO, as measured on a wire-bonded sample. The oscillator operates for varactor control voltages from 2 V down to 0.15 V, and has an oscillation frequency varying from 1.68 GHz up to 2 GHz, while using 20 mW from a 2 V power supply. The full set of characteristics of the VCO is depicted in Table 1.

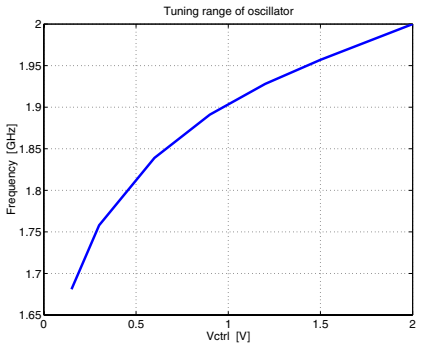

Figure 7: Tuning range of the on-chip VCO

Table 1: Measured VCO Specifications

Phase Noise @ 1 MHz for f_{osc}= 2 GHz	-128 dBc
Vdd	2 V
Tuning Range	17%
Center Frequency	1.84 GHz
Power Usage	20 mW

To demonstrate the linearity of the upconvertor and its usability for high bandwidth applications, measurements have been performed on a flip-chip bonded sample, driven by an external oscillator. For base band frequencies f_{BB} up to 33 MHz and an LO frequency f_{LO} of 2 GHz, the harmonic components at $f_{LO} \pm 2.f_{BB}$ and $f_{LO} \pm 3.f_{BB}$ are represented relative to the output power as *HD2* respectively *HD3* in Fig. 8. Similar results are obtained at LO frequencies of 900 MHz and 1.5 GHz. Also shown in this plot is the measured output power. For base band frequencies up to 16.7 MHz, the output power is larger than -12 dBm and up to 33 MHz the distortion is lower than -35 dBc.

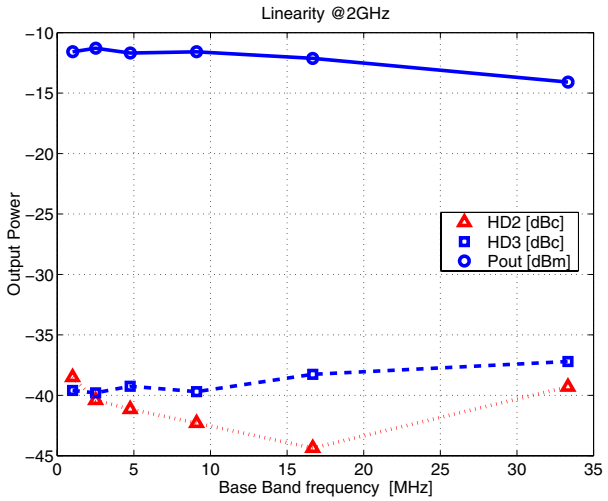

Figure 8: Output linearity and power vs. base band input frequency

A more common way to express output linearity is the use of OIP2 and OIP3. These can be derived from IM2 resp. IM3, being the second and third order intermodulation products relative to the power P_{Out} in the fundamental tone. By definition, OIP2(3) is the extrapolated value for P_{Out} that results in an IM2(3) of 0 dB in a plot of IM2(3) vs. P_{Out}.

Under conditions of low distortion (low power levels), following relationships hold [16]:

$$IM2 = 2HD2 \quad (1)$$

$$IM3 = 3HD3 \quad (2)$$

$$IM2 \propto P_{Out} \quad (3)$$

$$IM3 \propto P_{Out}^2 \quad (4)$$

From (1) and (2) it follows that IM2 and IM3 can be calculated from HD2 and HD3 by subtracting 3.0 dB resp. 4.8 dB from the measured distortion values. This method is used here as an approximation for two-tone measurements. Equations (3) and (4) show that one intermodulation (or distortion) measurement theoretically suffices to obtain a value for OIP2 and OIP3. However, for a linear mixer (4) is not valid for "low" values of the output power, according to [13]. Then, IM3 is proportional to P_{Out}.

Since measurements of HD2 and HD3 have been performed at one value of P_{Out} only, no decisive answer can be given to the question whether the measured P_{Out} should be regarded as "high" or "low". Therefore, Table 2 gives both theoretical values for OIP3. The "normal" one is indicated by $OIP3_3$ and the one valid for "low" power values in a linear mixer is indicated by $OIP3_2$. The value that would be derived from extrapolated measurements will be somewhere in between those values.

Table 2: Calculated values for OIP2&OIP3 @2GHz

f_{BB}	2.5 MHz	16.7 MHz	33 MHz
OIP2	26 dBm	29 dBm	22 dBm
$OIP3_3$	3.8 dBm	2.2 dBm	-0.3 dBm
$OIP3_2$	24.2 dBm	21.2 dBm	18.2 dBm

From the reasoning above, the representability of OIP3 as single number for the linearity performance of a linear mixer seems questionable. Moreover, an upconvertor will never be used at or in the region of the output power levels indicated by OIP2 or OIP3. However, the intermodulation or distortion at the maximum output power level of the upconvertor really is an important specification. Therefore, the measured harmonic distortion expressed as HD2 and HD3 is used to quantify the performance of this upconvertor. As already mentioned, values for IM2 resp. IM3 can be calculated from these distortion measurements using (1) and (2), respectively.

Table 3: Measured Specifications of the Transmitter

P_{BBin}		-3.5 dBm	
Vdd_{buffer}		2 V	
Vdd_{low}		1.3 V	
Noise floor @2GHz		< -133 dBc/Hz	
Power Usage @2GHz		25 mW	
F_{LO}[a]	HD2	HD3	P_{Out}
900 MHz	-34 dBc	-42 dBc	-10 dBm
1.5 GHz	-37 dBc	-42 dBc	-8.5 dBm
2 GHz	-44 dBc	-38 dBc	-12 dBm

[a]all measured for f_{BB}=16.7 MHz

In Table 3 the measured specifications for the upconvertor are summarized, using the same setup as above. For an f_{BB} of 16.7 MHz the distortion and output power at LO frequencies of 900 MHz, 1.5 GHz and 2 GHz are given.

8. CONCLUSION

In this paper, an upconvertor topology has been presented for which measurements show that base band signals with a bandwidth up to 33 MHz can be upconverted to RF frequencies up to 2 GHz in a standard CMOS technology. A passive high pass network is used to allow the upconversion to be done with a distortion low enough for higher order modulation schemes without the introduction of additional power drain. The power used by the upconvertor is lower than 25 mW. The test chip is shown to keeps its functionality at LO frequencies down to 900 MHz.

An on-chip VCO is capacitively coupled to a polyphase network that directly drives the mixer transistors. Thus, power-hungry buffering at RF-frequencies is avoided. The power consumption of the VCO is 20 mW. Specific circuit techniques and local optimization at circuit level of the building blocks have been used during design to obtain a global power minimization.

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