Analysis and Optimization of Substrate Noise Coupling in Single-Chip RF Transceiver Design

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Abstract: The relentless move toward single chip integration of RF, analog and digital blocks results in significant noise coupling effects that can degrade performance and hence, should be controlled. In this paper, we propose a practical methodology that uses a suite of commercial tools in combination with a high-speed extractor based on an innovative semi-analytical method to deal with noise coupling problems, and enable RF designers to achieve a first silicon-success of their chips. The integration of the methodology in a typical RF design flow is illustrated and its successful application to achieve a single-chip integration of a transceiver demonstrated.

1. INTRODUCTION:

The proliferation of Mixed-Signal-SOCs leads to two seemingly contradictory requirements on design methodology: on one hand, higher levels abstraction is needed to cope with the added complexity in design, while at the same time, the shrinking process technologies and the single-chip integration require inclusion of lower level details. The unprecedented impact of lower level physical effects such as interconnect parasitics, cross talk, as well as substrate bounce, IR drops, and inductance effects represent enormous challenges for electronics design automation (EDA) tool developers. Currently, designers are often forced to drift away from the physical phenomena at the transistor level to high-hierarchical levels, to be able to manage the increasing complexity of their designs. In this context, the potential of computer simulation in aiding the design decisions is becoming evident. For instance the relentless drive towards a single chip integration of digital and analog/RF sections has opened the door to a host of challenging noise coupling effects which should be controlled, and/or innovative design architectures are needed to achieve first-silicon success.

The switching activity of digital sub-circuits injects spurious signals into the substrate through the reverse junction capacitances or by impact ionization (hot carriers). Moreover, the transient current consumed, generates fluctuations in the internal supply voltage ($\Delta V=Ldi/dt$). These transient voltages can couple through metal lines and through the substrate to the sensitive parts of the chip corrupting their functionality by body effect or capacitive coupling. In addition, many side effects that corrupt the signal like: LO leakage, self mixing, DC offset, oscillator pulling and pushing are mainly due to the substrate coupling and supply noise. Moreover, phase noise [1-5], which leads to dramatic change in the frequency spectrum and timing properties is also enhanced by the switching noise that gets coupled to the Voltage-Controlled Oscillator (VCO) through the substrate from the high speed divider/counter circuit of Phase-Locked Loop (PLL) or from digital sub-circuits [4,5]. Currently, only RF front-ends with frequency synthesizer are sometimes integrated for such demanding applications as wireless phones. Efforts are underway, however, to integrate the entire transceiver for relatively undemanding applications such as RF identification systems and wireless local-area networks.

The principal strategies to limit substrate noise coupling are [6-9]:

- Using multiple pin assignment for power supplies/ground to reduce the value of the corresponding parasitic inductance
- Splitting supply lines and terminals of noisy and sensitive blocks
- Installing guard ring with dedicated on-chip ground
- Increasing the distances between noisy and sensitive circuits
- Using special package like ball-grid array package or flipchip
- Adopting differential topology for analog design
- Using silicon-on-insulator or triple-well technology

However, without the ability to analyze the true effects of substrate noise, many of these techniques are often over deployed, resulting in longer design cycles and increased manufacturing costs. Thus it is highly desirable to select the correct noise avoidance strategy to save valuable silicon area and avoid the use of costly process or packaging solutions. Many authors [10-15] have proposed useful techniques to the EDA tool developers, to improve the substrate modeling methods. However, without design-oriented methodologies that use efficiently these tools in the design flow, the substrate coupling problems will continue to lead to prolonged design cycles, and missed market opportunities.

In this paper, we propose a practical methodology that uses a suite of tools in an efficient manner to deal with substrate noise problems and enable RF designers to achieve an optimal integration and first silicon-success of their chips. The ultimate objective is to verify early in design flow if the noise coupling will corrupt the functions of the system. This condition enables us to make necessary design changes before physical implementation of the system, resulting in a significant reduction of the delay and the cost of the operation. However, the verifications at these stages are highly domain/circuit specific and can not be easily generalized nor automated. Nevertheless, a general strategy to guide designers in the early analysis can be elaborated. On the other hand, the substrate coupling is essentially a global problem that depends on full-chip layout, technology used, and package parasitics. Therefore, a strategy considering all these aspects in an iterative noise-immunity optimization loop, at full-chip level, is proposed. The methodology is integrated with a typical design flow: *Cadence* for layout and geometrical parameters, *Advanced Design System* for system and electrical simulations, and an improved *Boundary-Element-Method (BEM)* for a fast substrate modeling. We have chosen to improve BEM, because it is a semi-analytical method and thus lends itself to an adaptation to the physics of the specific problem much more readily than do pure numerical methods such as the *Finite-Difference Method (FDM)*. A successful application of the methodology to achieve a single-chip integration of a transceiver dedicated to ISM applications is illustrated.

2. EARLY VERIFICATIONS IN THE DESIGN FLOW

The cost of design correction grows exponentially as we go deeper in the design flow, and waiting till the full system implementation to verify

noise-coupling problems generates an unsupportable additive delay and cost. To deal with this problem, we focus on the development of a methodology that allows us to characterize the individual performances of the sensitive parts of the circuits in presence of substrate and supply noise. The methodology is entitled **SubCirI** and its flowchart is presented in Fig.1. The high level role of this methodology is to verify the RF front-end components separately, to make sure that they meet certain figures of merit specifications before putting them together. This methodology will enable us to make decisions during the circuit-level design. Its ultimate objective is to focus on the analog and RF parts which don't meet specifications in the presence of switching noise and which should be redesigned. The possibility of redesigning perturbing sections to generate less noise will also be considered. Eventually, the noise attenuation required to save the basic functionality of the system will be estimated. This information is very helpful to estimate the failure risk as a function of the technology and the package expected to be used. The blocks which meet specification with larger margin than required can also be relaxed, saving cost and power [16].
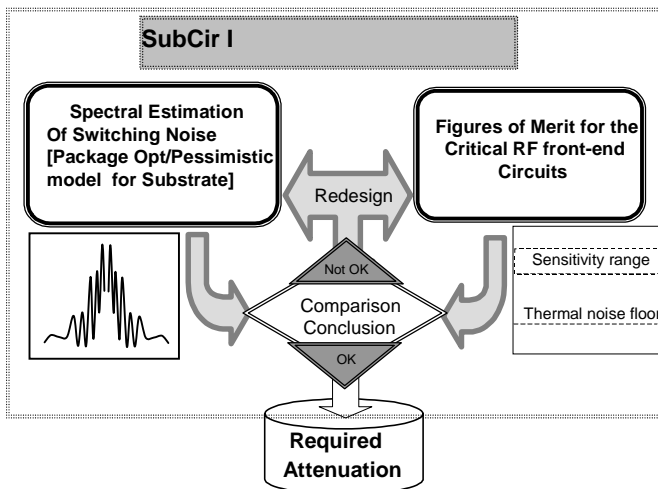

Fig. 1 Flow diagram of SubCirI methodology.

As shown in Fig.1, the successful construction of such methodology is only possible through a well-considered approach of three different aspects: the model of substrate and supply noise produced by perturbing circuits, the sensitivity to noise for analog and RF blocks and the estimation of the noise transfer functions from noisy blocks to sensitive parts. In our study, a worst case where the substrate is modeled as a single node, causing no attenuation of the noise between different placements of the chip is used. Therefore, we can verify if the RF front-end meets the figures of merit defined by the designers, even in presence of substrate noise and eventually determine which attenuation is necessary for this.

Several kinds of circuits can generate supply/substrate noise. In general, digital circuits are the noisiest parts of the chip. However, some analog cells, especially those with voltage/current transients or large signals such as power amplifiers, can be noise generators as well. For large circuits, the simulation at transistor-level, makes the exact switching noise evaluation very demanding in terms of memory and extraction time and even infeasible in several cases. To deal with this complexity, useful techniques have been proposed in the literature [17-22]. The methodology of [20], for instance, uses a macro-model library of digital cells that includes package parasitics, in combination with VHDL switching events simulation, to generate the transient noise of digital circuits. Because of the high-level nature of the method, it seems to be the more compatible approach for our SubCirI methodology. In the case of low and medium size perturbing
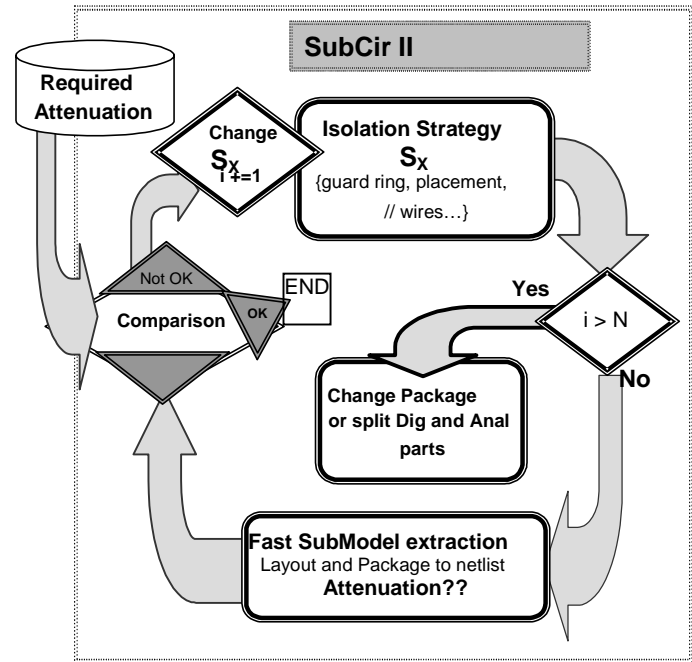

Fig. 2 Flow diagram of SubCirII methodology.

circuits, SPICE-like simulator is sufficient to simulate the power spectral density of their noise as will be seen in Section 5. On the other hand the principal impact of the noise on analog circuits is to limit the minimum signal that can be processed with acceptable quality and therefore, to limit their sensitivity. The key metric, characterizing the circuit performances in a noisy environment, is the signal to noise ratio (SNR). However, the variety and complexity of analog cells makes a unified physical explanation of how the noise affects their performances almost impossible. Our requirement of evaluating whether the analog RF functionality is corrupted, is only possible with an accurate transistor-level analysis of each potentially sensitive circuit separately. Many studies of noise impact on RF front-end blocks such as Mixers, VCO, LNA have been published [4-8], [23-25]. These works provide a very useful background for a successful application of SubCirI methodology.

3. METHODOLOGY FOR A FINAL VERIFICATION

Finally, when the layout of the circuit is completed, the methodology, **SubCirII,** described in Fig.2 is used. In this approach, we use the full package and substrate model in an iterative verification procedure of large varieties of isolation strategies. This methodology enables us to achieve better noise rejection for the circuit. We can also verify if we can meet the attenuation specified in SubCirI without changing the package or splitting the digital and the analog parts of the circuits.

The attenuation between sensitive and perturbing parts of the circuits depends essentially on substrate, package, and wire parasitics. For this purpose, we can use a suite of tools based on numerical finites-differences method (FDM). The base feature of the numerical method (FDM) is the high accuracy of the generated 3D-substrate model, since it can handle lateral and vertical resistivity variations and also arbitrary substrate geometry. The full chip simulation, however, makes the exact substrate coupling evaluation cumbersome. This problem is particularly critical for lightly doped substrate where the single-bulk-node model is not valid and a mesh over the entire substrate is necessary. Although sparse nonuniform grids can be used to speed up the extraction, an enormous amount of the surface mesh is necessary to match the full layout. Consequently, this approach is not suitable for the iterative method of Fig. 2, where the

verification and comparison of large variety of isolation strategies are necessary to achieve better noise rejection for our circuit. A thorough physical comprehension of the noise coupling effects with an improved Boundary-Element-Method (BEM) to accelerate the substrate model extraction and to avoid the dense matrix storage, however, will allow us to considerably simplify the problem, without any significant loss in accuracy, as will be proved in the following paragraphs.

a. Fundamentals of the Noise Coupling

Several investigations of the substrate noise coupling process were performed in order to capture their fundamental characteristics. As most CMOS logic elements can be reduced or decomposed into CMOS inverters, the designed substrate noise evaluation chip (Fig. 3) include *N* inverters with *N* varying from 12 to 1200.
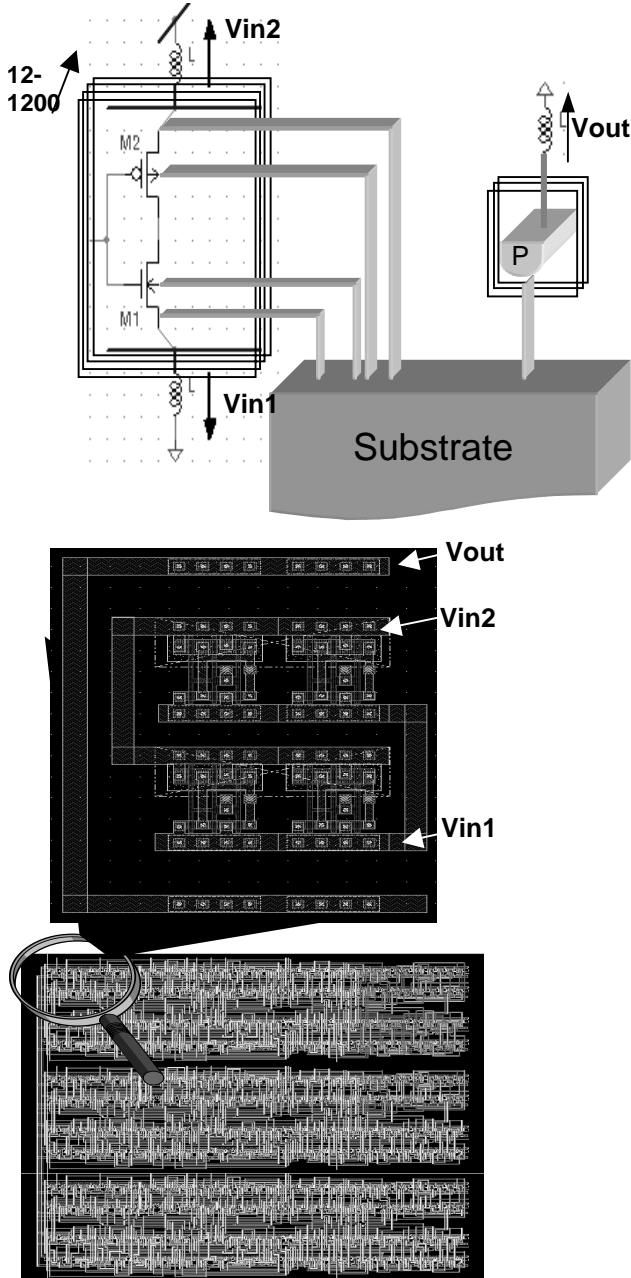

Fig. 3 Schematic and die photo of substrate coupling evaluation chip.

The transfer function *Vout/Vin1* and *Vout/Vin2* is simulated after including the full substrate model generated by *SubstrateStorm* [15] and a typical package parasitic (wire inductance = 5nH). As shown in Fig.3, *Vin1*, *Vin2*, and *Vout* are the on-chip ground node, the on-chip *Vcc* node of the circuit and an on-chip ground (GND) node representing a sensitive node respectively.

For lightly doped substrate (the standard technology in RF ICs), it is obvious that the metal connecting the ground/*Vcc* substrate contacts provides the lower impedance path to spurious signals. In addition, the power supply noise is generally several orders of magnitude higher than spurious currents injected through the Sources/Drains into the substrate [10]. As a consequence, our analysis will target the parasitic coupling between *Vcc*/ground contacts of the various blocks. On the other hand, the FET and bipolar transistors have a capacitance to the substrate in the range of few fF and $Z(1fF) \sim 1M\Omega$ (at 0.15GHz), which can be considered as infinite compared to typical substrate resistances. Consequently, we can predict that their presence around on-chip ground/*Vcc* contacts have no effects on the isolation between the ground/*Vcc* contacts. However, at the same time, the impedance of the transistors to substrate decreases at high frequency and for large circuits.

Therefore, the first questions that emerge are: according to these considerations can we consider only ground/*Vcc* contacts of the chip while formulating the substrate model, and what the limit of that model is in terms of frequency and number of transistors. To answer these questions, a simulation of the noisy-ground to sensitive-ground isolation (*Vout/Vin1*) is performed for a chip with 12 to 1200 inverters. For the *Simplified-SubModel* curves, only ground contacts of the layout were considered for substrate modeling. For the *Full-SubModel* curves, the substrate model of the full layout considering PMOS, NMOS, Wells, *Vcc* and Ground contacts was used. In both cases the netlist of the circuits were added to the substrate models to simulate the transfer functions. As shown in Fig.4, the simplified and full substrate models show excellent agreement for all frequencies and numbers of inverters considered. The reason is simple: the coupling path from *Vin1* to *Vout* can be decomposed into *N* parallel paths, and each path decomposed into an indirect paths through the NMOS ($R_t+1/j\omega C$) in parallel with a direct path through the substrate (R_s). The term ($1/\omega C+ R_t$) is much larger than R_s for two reasons: the low value of C (~fF) and high value of R_t (indirect path). In addition, even if the equivalent impedance of the *N* indirect path ($R_t+1/j\omega C$) decreases for large circuits (i.e. large *N*) the equivalent impedance of the *N* direct path (R_s) also decreases proportionally, and thus, remain the dominant coupling paths. Note that the package substrate system ($V_{out} \approx jL\omega/(R_s+jL\omega)$) becomes a high pass filter, with a corner frequency of *R/L*.
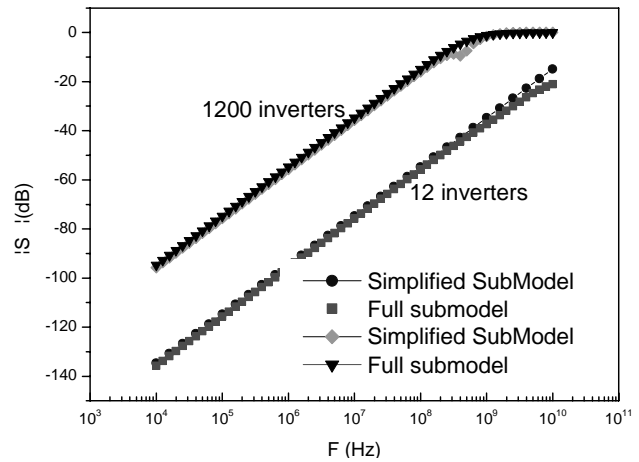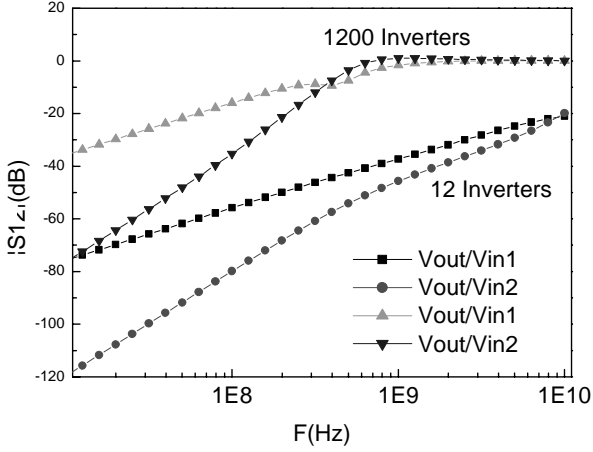

Fig. 4 On-chip ground-to-ground isolation (S=Vout/Vin1) for 12 and 1200 inverters as a function of frequency using simplified and full substrate models.

The second question now is: according to the fact that *Vcc* contacts are isolated using n-well in CMOS technology, can-we neglect *Vcc*-to-*Vcc* and *Vcc*-to-ground coupling and consider only ground contacts of the layout when we perform the substrate model? To answer this question, simulations of the noisy-*Vcc* to sensitive-ground isolation (*Vout/Vin2*) were performed for chips with 12 to 1200 inverters and compared with *Vout/Vin1*. The results are shown in Fig.5. In the high frequency range, the *S* values for ground-to-ground isolation (*Vout/Vin1*) are within the same order of magnitude as the *Vcc*-to-ground isolation (*Vout/Vin2*). Therefore, even if low frequency components of the power supply noise at *Vcc* are effectively filtered by well-junction capacitances, only the high frequency noise is attenuated. Hence, neglecting the *Vcc* and wells in the substrate model can lead to an underestimation of the noise effects.

Fig. 5 On-chip Vcc-to-ground isolation (Vout/Vin2) Vs ground-to-ground isolation (Vout/Vin1).

In conclusion, by considering only a layout with *Vcc*, ground contacts and wells for substrate model we can analyze and compare the isolation between various blocks of the circuits without any significant loss of accuracy and with a considerable gain in terms of execution time and memory used. Note that all these simulations were repeated for various positions of the inverters and sensitive contacts on the chip, and exactly the same conclusions were made.

b. Efficient Computation of the Substrate Model

In this section, we briefly describe the algorithm, used to extract the substrate model. The method is based on an improved Boundary-Element-Method (BEM) [10]. In fact, the substrate Green's function G and the elements z_{ij} of the impedance matrix that relates the currents (I_j) and potentials (ϕ_i) of all panels of the layout has been previously computed in an analytical form [11] and shown to be

$$z_{ij} = \frac{\overline{\varphi_i}}{I_j} = \frac{1}{s_i s_j} \int_{s_j} \int_{s_i} G(s_i, s_j) ds_j ds_i \; ; \; G = \sum_{m,n=0}^{\infty} \left\{ \begin{array}{c} f_{mn} \cos\left(\frac{\alpha x}{a}\right) \cos\left(\frac{\alpha x'}{a}\right) \\ \cos\left(\frac{\beta y}{b}\right) \cos\left(\frac{\beta y'}{b}\right) \end{array} \right\}$$

(1)

Where $\alpha = m\pi/a$, $\beta = n\pi/b$, a and b are the substrate lateral dimensions, S_i and S_j denote the surfaces of the panels i and j. Here, f_{mn} is computed using recursion formulas as shown in [11]. It is also demonstrated in [11] that z_{ij} can be expressed as a function of 64 2–D discrete cosine transform (DCT) coefficients ($K(p,q)$), with

$$K(p,q) = \sum_{m=0}^{P-1} \sum_{n=0}^{Q-1} k_{mn} \cos\left(m\pi \frac{p}{P}\right) \cos\left(n\pi \frac{q}{Q}\right)$$

(2)

k_{mn} is a function of f_{mn}, and the *64 (p , q)* terms are determined from the ratio of contact coordinates and substrate dimensions. A high-speed computation of these coefficients can be made using the fast Fourier transform, FFT [11]. Once the impedance matrix Zp is computed, one needs to invert it in order to generate the admittance matrix Yp.

The time and memory hungriest step in BEM is the storage and inversion of the impedance matrix. In general, the matrix Zp is very dense and its inversion involves such a considerable effort that it is difficult to handle problems with a large number of contacts. Iterative algorithms such as the *Generalized Minimum Residual* algorithm, GEMRES can be used to speed up the computation. It's worth noting that the substrate model generated by BEM, like any electromagnetic model, often introduces physical errors, since it is only an approximate representation of the reality. Beyond that, an exact numerical solution is rarely accessible, adding a further numerical modeling error. Some precautions can be taken to limit these errors. For instance, to use FFT, we use a decomposition of substrate dimensions in $P \times Q$ elements and assume that

$$K(p,q) = \sum_{n=0}^{\infty} \sum_{m=0}^{\infty} \ldots \cong \sum_{n=0}^{P} \sum_{m=0}^{Q} \ldots$$

(3)

The use of higher values for P and Q improves the accuracy of this assumption, but at the same time increases the computational cost. In general, the limit values for P and Q that we can use with a reasonable computational effort is 1024 (2^{10}). However, by decomposing the summations and exploiting the symmetry characteristics of the DCT (i.e. $cos[(m+2JP)\pi p/P] = cos[m\pi p/P]$), it is possible to get larger number of coefficients, that is $(J+2)P(J+2)Q$ with an arbitrary J, without significant additional cost. In fact we can demonstrate after some algebra that

$$\begin{aligned} K(p,q) &= \sum_{m=0}^{(J+2) \times P-1} \sum_{n=0}^{(J+2) \times Q-1} k_{mn} \cos\left(m\pi \frac{p}{P}\right) \cos\left(n\pi \frac{q}{Q}\right) \\ &= \sum_{m=0}^{P-1} \sum_{n=0}^{Q-1} K_{Jmn} \cos\left(m\pi \frac{p}{P}\right) \cos\left(n\pi \frac{q}{Q}\right) \end{aligned}$$

$$\text{with} \quad K_{Jmn} = \sum_{k=0}^{J} \sum_{i=0}^{J} \left\{ \begin{array}{c} k_{\substack{m+2kP \\ n+2iQ}} + k_{\substack{m+2(k+1)P \\ n+2(i+1)Q}} (-1)^p (-1)^q + \\ k_{\substack{m+2kP \\ n+2(i+1)Q}} (-1)^p + k_{\substack{m+2(k+1)P \\ n+2iQ}} (-1)^q \end{array} \right\}$$

(4)

On the other hand, the implementation of BEM leads to a numerical instability problem. The problem comes from the formulation of k_{mn} published in [11], which, with finite precision machine evaluation, results in unacceptable values (0/0) during the computation. A numerically stable green function in the case of 3D arbitrary arrangement of contacts is proposed in [12]. The adaptation of this technique to our case gives

$$k_{mn} = \frac{a^2 b^2 f_{mn} C_{mn}}{m^2 n^2 \pi}$$

(5)

with

$$f_{mn} = \frac{1}{ab\sigma_N \gamma_{mn}} J_N \; ; \; J_k = \frac{J_{k-1} + \frac{\sigma_{k-1}}{\sigma_k} \tanh\left(\gamma_{mn}(d_k - d_{k-1})\right)}{J_{k-1} \tanh\left(\gamma_{mn}(d_k - d_{k-1})\right) + \frac{\sigma_{k-1}}{\sigma_k}}$$

and $\quad J_0 = \tanh\left(\gamma_{mn} d\right)$

(6)

Here σ_k and d_k are the conductivity and coordinate of each substrate layer respectively. More details on the C_{mn}, γ_{mn} can be found in [11]. We can

also force GEMRES to converge to very tight tolerances, to avoid the loss of information, during the inversion process. Despite all these precautions, BEM continues to have difficulties to handle large circuits. In fact, for a design with a large number of contacts, the admittance matrix elements y_{ij} corresponding to the geometrically distant panels become extremely weak, especially for high-resistivity substrate and when the number of panels between i and j is significant. At the same time, the y_{ij} elements corresponding to neighboring panels are very large. In this context, the unavoidable physical and numerical errors, even if made very small, lead to wrong results and even non-physical values for a number of low Yp elements and for the corresponding resistances. The problem becomes more acute, when the number of contacts increases.

As demonstrated in the previous section, a layout with wells, *Vcc*, and ground contacts, is sufficient to have an accurate representation of the inter-block substrate coupling. Despite these simplifications of the layout, the resulting network remains too dense to enable the targeted full-chip analysis. Therefore, further modification in numerical methods has been made in order to reduce computational efforts. The crucial observation we make here is that the ground substrate contacts (or *Vcc* contacts) of each block of the chip are linked by metal lines. Hence, all substrate coupling paths between them are shorted. We can, therefore, consider the ground contacts (or *Vcc* contacts) of each block (supposed to have its own on-chip ground) as a single contact while performing inter-block substrate coupling. Consequently, the discretization explained in Fig. 6 is sufficient for an accurate inter-block coupling representation. In fact, since we focus on the coupling path between the various blocks of the chip, we can consider that the currents at the contacts positioned near the edges of each block are very high, compared to the currents at the contacts situated in its center. Therefore, the edge contacts are the most dominant coupling paths between blocks. This is the reason why a fine partition should be used in the edge regions. As we move towards the center of the block, the role of the contacts in the inter-block coupling becomes progressively weaker, and hence, we can use increasingly coarser partitions. The currents at the ground contacts (respectively *Vcc* contacts) of each partition are considered to be constant.

The question that emerges now is: how to exploit this partition to speed up the numerical computation? Let us consider two partitions of the chip i and j, having L and M number of contacts respectively (Fig. 6).
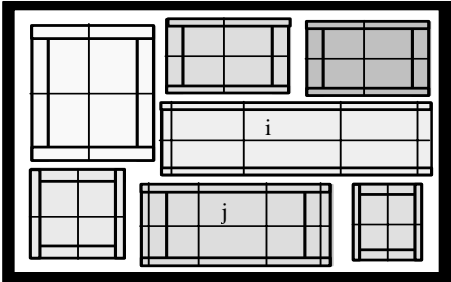
Fig. 6 Chip partitioning for inter-block coupling analysis.

Since we assume that the currents of the L contacts (and the M contacts) are constant, the impedance z_{ij} representing the substrate coupling between the two partitions can be defined as

$$z_{ij} = \frac{\overline{\varphi_i}}{I_j} = \frac{\overline{\varphi_j}}{I_i} = \frac{1}{\sum_{l=1}^{L} s_l \sum_{m=1}^{M} s_m \sum_{l=1}^{L} s_l \sum_{m=1}^{M} s_m} \int_{S_l} \int_{S_m} G(s,s') ds ds'$$

(7)

S_l and S_m are the surfaces of each contact in the partitions i and j (l ε [1,L] and m ε [1,M]), G is the Green's function of the substrate, $I_{i,j}$

and $\phi_{i,j}$ are the current and the potential of the contacts in panels (i and j) respectively. From a decomposition of the integrals on each contact within the partitions i and j, we obtain

$$z_{ij} = \left(\sum_{l=1}^{L} s_l \sum_{m=1}^{M} s_m \right)^{-1} \sum_{l=1}^{L} \sum_{m=1}^{M} \int_{S_l} \int_{S_m} G(s,s') ds ds'$$

(8)

The double integrals in this equation represent the impedance between the contact l of partition i, and contact m of partition j. Thus z_{ij} can be represented by a sum of impedances between the contacts of each partition as

$$z_{ij} = \sum_{l=1}^{L} \sum_{m=1}^{M} z_{lm} s_l s_m \Bigg/ \sum_{l=1}^{L} \sum_{m=1}^{M} s_l s_m$$

(9)

Using the same procedure with some algebra, we can relate z_{ii} to the impedance between the contacts of the partition i. Thus, we obtain

$$z_{ii} = \left(\sum_{l=1}^{L} s_l^2 \right)^{-1} \left(2 \times \sum_{l=1}^{L} \sum_{j=l+1}^{L} z_{lj} s_l s_j + \sum_{l=1}^{L} z_{ll} s_l^2 \right)$$

(10)

As mentioned earlier, the time hungriest step in BEM is the storage and inversion of the impedance matrix. Our algorithm transforms this impedance from a matrix of M^2 elements, with M the number of contacts, to an impedance matrix of P^2 elements, with P as the number of partitions. Therefore, the gain in computational cost is evident.

We would like to point out that the inversion of the matrix, without partitioning simplification, is problematic for another extremely important reason. The admittance matrix elements that we would compute are very heterogeneous. The y_{ij} corresponding to the geometrically distant panels are very small, especially for high-resistivity substrate and when the number of panels between the i and j is significant. At the same time, the y_{ij} elements corresponding to neighboring panels are very large. The system matrix that results is ill-conditioned. In this context, the unavoidable physical and numerical errors, although small, can lead to wrong results and even non-physical values for a number of low y_{ij} elements. The meshing strategy resolves the problem due to the following three effects: first, the number of matrix entries is significantly reduced, which decreases the numerical inversion errors; second, by choosing the edge meshing to be sparser than the center one, the large elements of the current density vector near the edges are compensated by smaller area, so that more uniform total current vector is obtained; and thirdly, by decreasing the number of effective contacts that can exist between geometrically distant ones, we reduce the probability of having very weak y_{ij} elements.

4. CASE STUDY

The first purpose of this study is to show how to use the methodology, SubCirI, to help a single-chip integration of a BiCMOS super-regenerative transceiver dedicated to ISM applications [26-27]. The substrate used is lightly doped with a resistivity of 20 Ω-cm. The basic block diagram of a super-regenerative receiver is very simple (see Fig. 7): the RF input is connected to an Isolation Amplifier, followed by a gain stage connected in closed loop with a selective network. This stage represents an oscillator whose startup time depends on the RF signal at the input. The gain of the amplifier is periodically modified below and above the critical oscillating conditions by the quench signal and the demodulation is achieved through detection of the envelope of the output signal of the oscillator. The transmitter is based on the oscillator of the receiver. This oscillator, which is followed by a Power Amplifier (PA), is able to deliver a minimum of 0dBm to a differential load. In this design the Power Amplifier, with its associated bond-path and wires are the strongest transmitters of cross-talk.

In the first designed version, an off-chip load-resonant (without the on-chip capacitors C_0: version1 Fig.7) is designed to restore a 916 MHz sinusoidal voltage at the antenna and suppress their higher harmonics. A fully differential design is used to minimize the substrate noise injection and the transient currents in the power supply. However, the oscillator is the best receiver of cross-talk and even a low noise coupling from the PA can results in its malfunction and therefore the instability of the system.
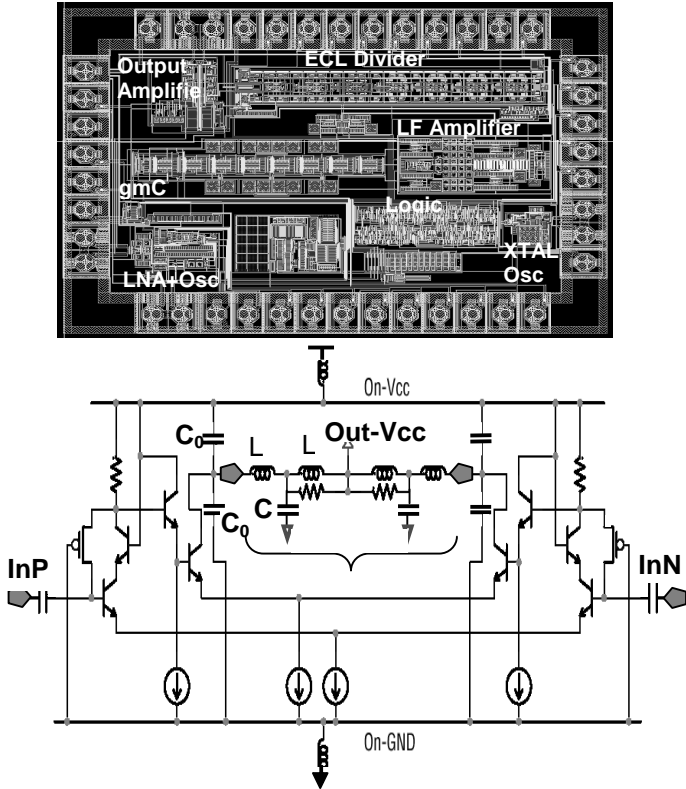

Fig. 7 The Transceiver Chip and PA schematic
Version 1(Load 1 with only off-chip C):C=5.5 pF; L = 5 nH;R=300 Ω.
Version 2(Load 2 with only on-chip C_0):C_0 = 2pF;L=5nH;R=300 Ω.

According to our methodology (Fig.1), we focus on the oscillator as the potential "listener" and the PA as the possible "talker". The oscillator is designed to have less than –100 dBc/Hz of phase noise at 500KHz offset. Generally, to meet the Federal Communication Commission (FCC) regulation, the 902-928 MHz ISM band is partitioned into 54 channels, requiring a frequency resolution of 482 KHz in the synthesizer [29]. In our design, to preserve the required SNR in the adjacent channels, we specify a certain spectral purity with spurious tones below –70dBc at 482KHz offset from the carrier. In the oscillators, the environmental noise translates to spurs by frequency modulation FM phenomena. In fact, the noise corrupts the dc voltage applied across the varactors, and varies the tank capacitance and hence the resonance frequency. Viewed as analog FM, this effect translates low-frequency noise components in the control path to region around the carrier [4]. The example of spurious tones generated by a 0.01V/1MHz signal at the control path of our oscillator is shown in Fig. 9 (a). Therefore, by applying sinusoidal signals with various amplitudes and frequencies at the control path, we can determine the maximum amplitude that the oscillator can tolerate without generation of FM spurs higher than –70 dBc beyond 482 KHz offset from the carrier. To compare these signals to power spectral density (PSD) of the PA noise, their amplitudes will be translated to a power spectrum. The results are represented in Fig.8 (b). The PA noise generated at its on-chip ground and its PSD is

represented in Fig.8. The peak-to-peak noise reaches its maximum (0.14V) when the PA switches from off-mode to on-mode. The PSD of the noise indicates that most of the spectrum is located around 1.8GHz (twice the input/output frequency). This is due to the differential topology of the PA. In low frequency (LF) range, the PSD of the noise is around –37 dB. The maximum tolerated noise in the control path of the oscillator is, however, in the range of –60 to –40 dB as shown in Fig. 9. Therefore, the PA generates a supply noise PSD of 3 to 23 dB higher than the maximum tolerated by the oscillator.
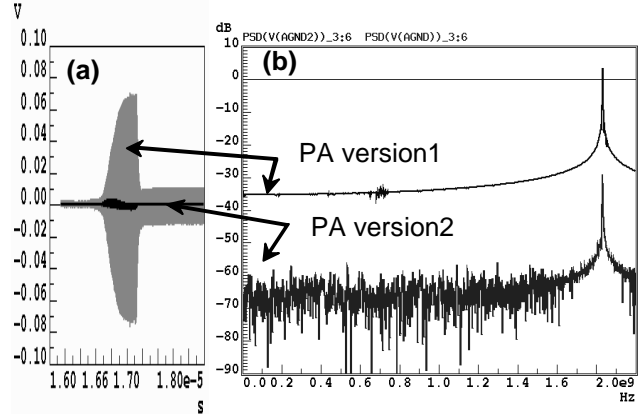
Fig. 8 a) PA noise waveform and b) its PSD.
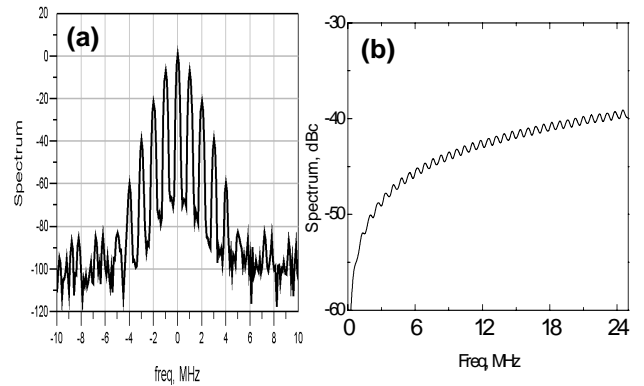
Fig. 9 a) Spectrum of spurious tones generated by a 0.01V/1MHz signal at the control path of the oscillator b) The maximum tolerated noise PSD by the oscillator to have an out-of-channel spurs lower than –70 dBc.

To preserve the functionality of our system we have the choice between two solutions: redesign the PA to generate less noise or add a voltage regulator circuit to the oscillator with bandgap reference to decouple the VCO and its control path from on-chip power supply. It is obvious that the first solution is the best, since it provides a quiet environment and therefore avoids the corruption of other circuits by the PA noise.

The method proposed to avoid the generation of the high frequency noise at the bond wires is based on the exploitation of the filtering properties of the load-resonant. In fact, coupling the on-chip ground and Vcc to the outputs of the PA using the on-chip capacitances C_0 (Fig.7) instead of the use of the off-chip C, results in a significant decrease in the on-chip ground and Vcc impedances. The schematic of the redesigned PA according to this technique is shown in Fig.7 (PA version 2). The peak to peak noise at on-chip ground, which is proportional to this impedance ($\Delta V \approx Z_L \, di/dt$), is therefore, strongly reduced. To avoid the generation of low frequency noise, an on-chip ground different from that of the circuit, is used to bias the substrate. The low transistor junction capacitances between the noisy ground of the circuit and the substrate contacts strongly

attenuate the low frequency noise. The noise PSD generated by the PA at LF range is reduced from -37dB for PA version 1 to -70dB for PA version 2 as shown in Fig. 8, and thus becomes lower than the maximum noise tolerated by the oscillator.

Finally, during the physical implementation of the various blocks, we can start the application of methodology SubCir II. As mentioned in the introduction, several noise-transfer reduction techniques are reported in the literature. Usually the efficiency of these techniques depend on the design parameters, such as the resistivity of the substrate, the bond-wires inductance values, the frequency of the noise etc.

	K(p,q)	Fast BEM	FDM
Runtime User+Sys.	1mn 14 s	4mn 24s	1h 30mn 40s

Table I : Runtime comparison between the extractions methods (FDM and FastBEM) for each iteration of SubCirII.

In this paragraph, we show how the methodology SubCirII allows us to verify and compare the efficiency of the various strategies and to achieve the optimal quiet noise environment for our circuit. To speed up the substrate model extraction, and therefore to enable an iterative verification of these strategies, the simplified model (outlined in Section 3a) that takes into account only the coupling between ground taps is used. Note that, since the technology used is BiCMOS, the amount of *Vcc* substrate contacts is very low and have negligible effects on substrate coupling. The layout of the transceiver is represented in Fig. 7. Both the FDM and the improved BEM (FastBEM) were used for the substrate modeling in each iteration. Similar results between the FDM and the FastBEM techniques were found as shown in Fig.10 (continuous lines for FDM and dotted lines for BEM). However, the time and memory gain is considerable when we use the improved BEM as illustrated in Table I.
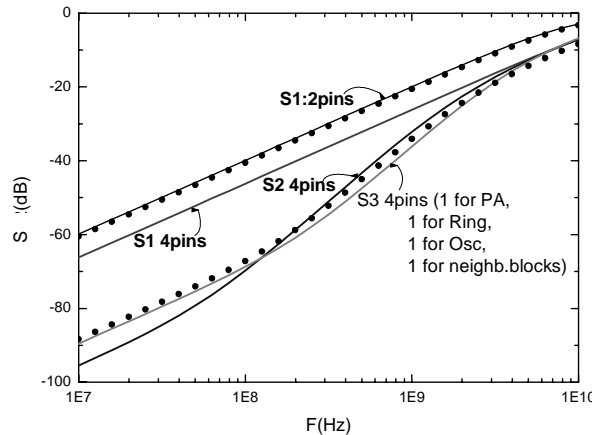
Fig.10 Comparison between the results of S1, S2 and those of the adopted strategy for the final design, S3. The extractions are performed both by the improved BEM (dotted lines) and by the FDM (continuous lines).

The first visited strategy by the loop (named S1) consists of the increase of the number of the package pins and wires. The second strategy (S2) consists of the use of separate on-chip grounds for the Oscillator-LNA and the rest of the circuit. The effect of S1 is illustrated by solid lines (Fig.10): top curve for 2 pin-wires (One for the PA and one common pin for the Oscillator-LNA and neighboring blocks-peripheral to the circuit), and bottom curve for 5 pin-wires (one for the PA and 4 common pins for the Oscillator-LNA and

neighboring blocks-peripheral to the circuit). The isolation is improved by about 16 dB when the number of package pins is increased from 2 to 5. This is mainly due to the reduction of the bond-wire inductance value, which results in an on-chip GND close to the external reference (off-chip GND). Beyond 5 package pins, the improvement of the isolation becomes negligible. In addition, this improvement is practically independent of the frequency. The effect of S2 is illustrated by the dotted line. For the same number of package pins (that is 4), the separation of the GND improves the isolation by 25 dB at 100 MHz and 10 dB at 1 GHz in comparison to S1. In addition, it is verified that the improvement due to the increase in the number of pins is negligible when the on-chip grounds are separated.
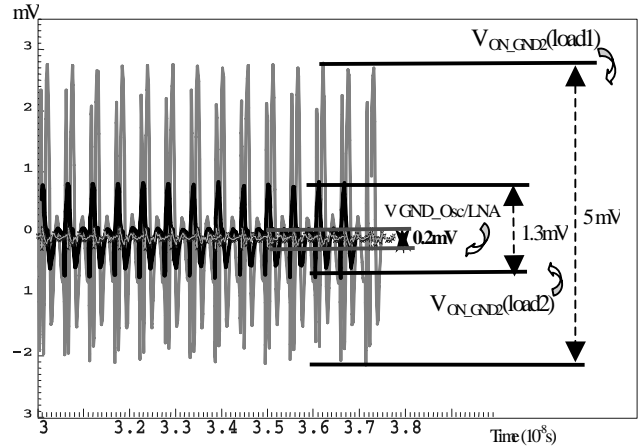
Fig. 11 Noise waveform at the on-chip ground used to bias exclusively the substrate for the two versions of the PA (V_{ON_GND2}(Load1/2)), and the noise waveform detected at the GND of the oscillator (V GND_Osc/LNA).

The strategy adopted for the final iteration is S3. It consists of placing and biasing guard rings. Compared to S2, for the same number of pins (that is 4); the placement of a guard ring, with dedicated pins, around the amplifier allows a significant improvement at high frequency (10 dB at 1GHz) as shown in Fig.10. It should also be noted that this result is practically independent of the size of the guard ring. The improved design of the PA (Fig. 7) is combined with the isolation strategies S3, to ensure a quiet environment for the oscillator. The results are illustrated in Fig .11. The waveform of the noise detected at the ground of the oscillator after applying strategy S3 is also represented by the curve $V_{GND\_Osc/LNA}$ in the same figure. It is evident that the combinations of the PA low noise supply technique and the optimal isolation strategy S3 lead practically to the elimination of substrate noise coupling in our circuit. The performances of the final version of the transceiver were found to be in agreement with the initial specifications. The measured transmitter current with an output power of 0dBm on a 300 Ω resonant load is 6 mA. The maximum operating frequency measured with a chip-on-board technology is 1.5 GHz.

5. CONCLUSION

In this work we have focused on the development of methodologies for the analysis and optimization of substrate noise effects in mixed-signal circuits. Two methodologies were elaborated: one for an early design verification, and another for a final verification/optimization of the noise immunity of the circuits. A new approach, which combines a thorough physical comprehension of the noise coupling effects and an improved version of the BEM, to accelerate the substrate model extraction and enable the use of the iterative optimization procedure is proposed. These methodologies have been successfully employed to verify the functionality of the components of an RF system, and to make sure that they meet the specified figures of merit before being assembled together. The redesign of

the PA results in a reduction of low frequency spurs around the carrier by about 30dB. The iterative optimization procedure enables us to increase the isolation between the noisy PA and the sensitive oscillator, by about 40dB in medium frequency range and 30dB around 1GHz.

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