MEDEA+ and ITRS Roadmaps

J. Borel, STMicroelectronics
G. Matheron, MEDEA+ Office
A. Jerraya, TIMA
S. Resve, UC Berkley
M. Rogers, Intel
W. Rosenstiel, FZI and Univ. of Tübingen
I. Rugen-Herzig, Infineon Technologies
F. Theewen, Philips Research Labs

The ITRS Technology Roadmap recent revision has shown again an acceleration of the Very Deep Submicron process availability with design capabilities forecasted in hundred millions of gates per square centimeter in 2010.

This will again raise the question on how to cope with such complexities and functionalities (A-D,HW-SW, MEMS…) in EDA solutions.

In this panel will be discussed what are the main priorities in EDA as seen through the applications specificities in USA (ITRS-2001 DESIGN ITWG) and in Europe (The MEDEA EDA Roadmap).

The panelists will present the strategies in their respective fields of interest, resulting from their working groups conclusions. They will underline the breakthroughs and potential developments of solutions and the milestones to reduce design times and increase design quality.

The focus will be on application driven solutions, mostly in the SoC domains (covering both hardware, embedded and application software).