Systematic Design of a 200 MS/s 8-bit Interpolating/Averaging A/D Converter

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ABSTRACT
The systematic design of a high-speed, high-accuracy Nyquist-rate A/D converter is proposed. The presented design methodology covers the complete flow and is supported by software tools. A generic behavioral model is used to explore the A/D converter's specifications during high-level design and exploration. The inputs to the flow are the specifications of the A/D converter and the technology process. The result is a generated layout and the corresponding extracted behavioral model. The approach has been applied to a real-life test case, where a Nyquist-rate 8-bit 200 MS/s 4-2 interpolating/averaging A/D converter was developed for a WLAN application.

Categories and Subject Descriptors
B.7.m Integrated Circuits: miscellaneous

General Terms
Design

Keywords
A/D converters, Interpolating, Flash, Simulated Annealing.

1. INTRODUCTION
In the design of analog functional blocks as part of a large system on silicon, a number of phases are identified. These are depicted in Fig. 1. The first phase in the design is the specification phase. During this phase, the analog functional block is analyzed in relation to the surrounding system to determine the system-level architecture and the required block specifications. With the advent of analog hardware description languages (VHDL-AMS, VERILOG-A/MS), the obvious implementation for this phase is a generic analog behavioral model [1]. This model is parameterized with respect to the specifications of the functional blocks. A list of specifications is given in Table 3 later on. The next phase is the design (synthesis) of the functional block. It consists of sizing & layout and is shown in the center of Fig. 1. The design methodology used is top-down performance-driven [2]. This design methodology has been accepted as the de facto standard for systematically designing analog building blocks [2]. Finally, a behavioral model for the block is extracted from the sized circuit including (layout) parasitics. This allows verifying and efficiently simulating the block as part of a larger system. This methodology is now applied to an interpolating/averaging A/D converter.

The paper is organized as follows. Section 2 explains the chosen A/D converter architecture. Section 3 describes the systematic design methodology in detail and section 4 presents the measurement results. Finally, conclusions are drawn in section 5.

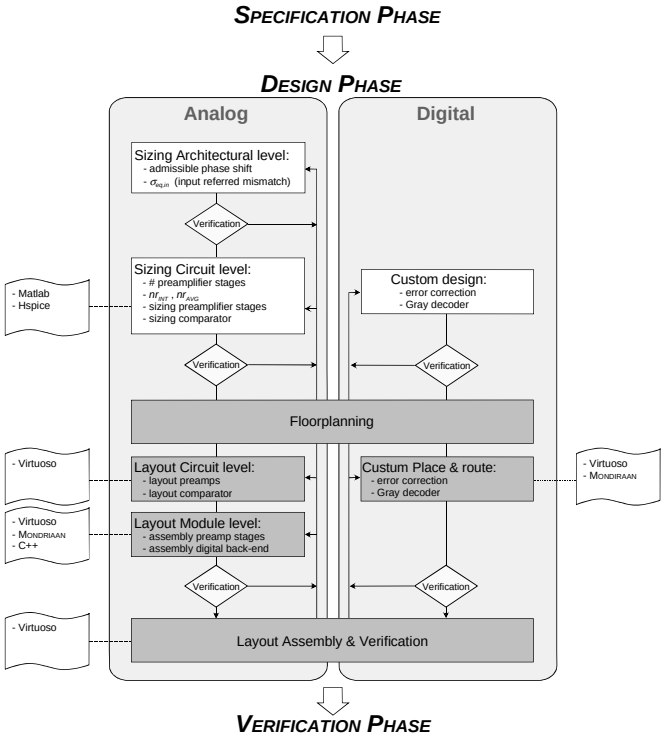

Figure 1: Presented systematic design flow for an interpolating/averaging A/D converter.

2. THE INTERPOLATING/AVERAGING ARCHITECTURE
The interpolating/averaging architecture is shown in Fig. 2. Just as in the flash architecture, processing is fully parallel resulting in high sampling rates [3]. The front-end is fully differential for improved dynamic performance. A Sample & Hold circuit (S/H) samples the differential input signal. The resulting signal is compared with the fully differential reference ladder network and amplified in the first amplification stage. The output of this

DAC 2002, June 10-14, 2002, New Orleans, Louisiana, USA.

preamplifier stage is interpolated $nr_{INT,st1}$ times. A second preamplifier stage is added, which is interpolated $nr_{INT,st2}$ times. Both preamplifier stages use averaging to improve static performance [4]. The outputs of the preamplifier stage(s) steer the regenerative comparators. A digital back-end performs additional error correction (e.g. against bubble errors) and encodes the thermometer coder output from the comparators in Gray code, which is synchronized at the output by a latch.

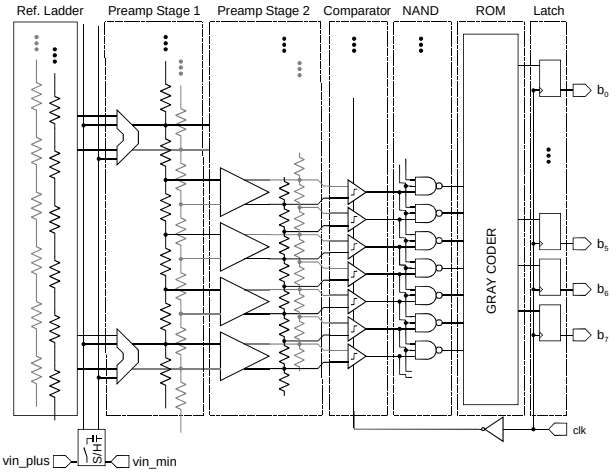

Figure 2: Block diagram of the interpolating/averaging A/D converter architecture.

Table 1: List of designable parameters for the proposed interpolating/averaging A/D converter.

	Designable parameters
Architectural level	Phase shift at Nyquist frequency
	Input referred offset $\sigma_{total,offset}$
Circuit level	Resistance reference ladder R_{ladder}
	Boost voltage S/H
	$(W,L)_i$ tors S/H
	Level of interpolation: $nr_{INT,st1}$ / $nr_{INT,st2}$
	Amount of averaging: $nr_{AVG,st1}$ / $nr_{AVG,st2}$
	Resistance for averaging: $R_{AVG,st1}$ / $R_{AVG,st2}$
	Gain preamps: $A_{preamp,st1}$ and $A_{preamp,st2}$
	$(W,L)_i$ transistors preamps
	Regeneration time constant τ_{reg}
	$(W,L)_i$ transistors comparator
	$(W,L)_i$ transistors digital back-end

3. SYSTEMATIC DESIGN OF THE A/D CONVERTER

3.1 Specification phase.

Two approaches are available for the statistical behavioral modeling of A/D converters: equation-based modeling [5] or macro modeling [1]. This equation-based approach has the advantage that Monte-Carlo simulations are no longer needed and thus simulations can be speeded up considerably. For timing verification/simulation though, macro models are better suited. To study the effects of clock jitter, signal dependent delay, etc. the designer needs to resort to macro-models as presented in [1]. In the presented approach these macro models were used.

3.2 Design phase

The specifications derived during the system-level specification phase are now the input to the converter design phase. The design of the converter is performed hierarchically. The design parameters are listed in Table 1. First, some architectural decisions have to be made. Both static and dynamic performance are taken into account, resulting in specifications for mismatch and admissible phase shift for the different building blocks.

3.2.1 Architectural-level sizing.

A Monte-Carlo simulation can be used to estimate the design yield as a function of the total equivalent input-referred offset [10]. For these simulations a targeted INL of 1.0 LSB and a targeted DNL of 0.5 LSB were used. Using averaging techniques, the DNL can be improved by a factor of nr_{AVG}, while the INL can be improved by $\sqrt{nr_{AVG}}$ [4], resulting in the plot shown in Fig. 3. The yield is plotted as a function of the offset, with the amount of averaging nr_{AVG} as a parameter varying from 1 (i.e. no averaging) to 9. With e.g. an averaging of 9 (nr_{AVG} =9) the simulations yield a constraint for the admissible total equivalent input-referred offset:

$$\sigma_{total,offset} \leq 0.7\ LSB \qquad (1)$$

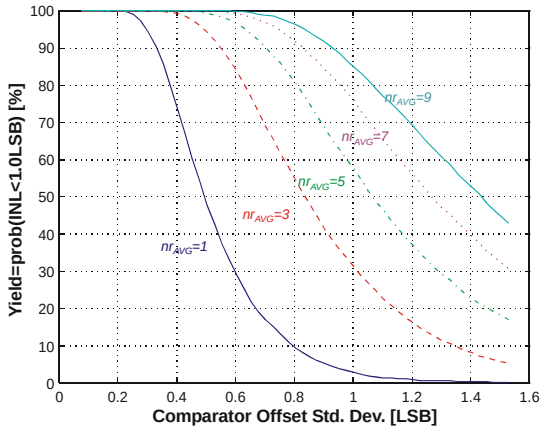

Figure 3: Estimated yield as a function of the total equivalent input referred offset for a targeted INL of 1.0 LSB.

From Fig. 2, the total equivalent input-referred offset $\sigma_{total,offset}$ can be calculated as:

$$\sigma^2_{total,offset} = \sigma^2_{preamp\_st1,offset} + \left(\frac{\sigma_{preamp\_st2,offset}}{A_{preamp\_st1}}\right)^2 + \left(\frac{\sigma_{comp,offset}}{A_{preamp\_st1} \cdot A_{preamp\_st2}}\right)^2 \qquad (2)$$

where $\sigma_{preamp\_st1,offset}$ is the input-referred offset of the preamplifier stage 1, $\sigma_{preamp\_st2,offset}$ is the input-referred offset of the preamplifier stage 2, and $\sigma_{comp,offset}$ is the input-referred offset of the comparator stage. The latter term is negligible if the gain in the preamplifiers is high enough. From statistical behavioral modeling [1] and technological constraints of the process used (0.35 µm CMOS), it can be calculated that a total gain of 15 is sufficient for the comparator to have negligible contribution in the total equivalent input-referred offset.

$$A_{preamp} = A_{preamp\_st1} \cdot A_{preamp\_st2} = f(INL, technology) \geq 15 \quad (3)$$

In this design A_{preamp} was chosen 20. Thus mismatch and speed no longer have to be traded off for the comparator, allowing to optimize the comparator for speed.

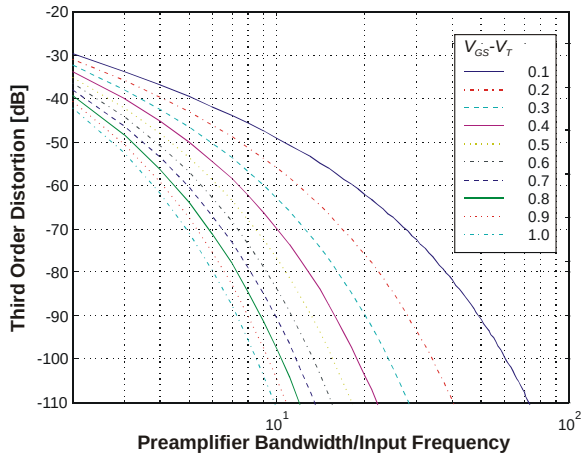

Figure 4: HD_3 as a function of the preamplifier bandwidth/input frequency ratio for a V_{fs} of 1.25 V.

Apart from the mismatch constraint, the admissible phase shift for the preamplifier is also determined at this stage of the design. In [3] a formula was derived for the resulting third-order distortion HD_3 as a function of the bandwidth of the preamplifiers:

$$HD_3 \approx \frac{2g}{3\pi}\frac{f_{in}}{f_b}, \text{ where } \quad g \approx e^{-2b_n \frac{(V_{GS}-V_T)}{V_{fs}}\frac{f_{in}}{f_b}-1} \quad (4)$$

V_{fs} is the full-scale input range, f_{in} is the input frequency and f_b is the bandwidth of the preamplifier, g represents the normalized delay $\delta t_d/BW$ of the preamp, b_n is the relative output level. The normalized delay is worst-case around the mid-codes i.e. when $b_n = 0.5$. The results of equation (4) are depicted in Fig. 4: for this example the targeted 50 dB distortion would result in a constraint of 10° phase shift at Nyquist frequency for a V_{GS}-V_T of 0.3 V:

$$\varphi_{Nyquist} \leq \text{atan}(1/6) \approx 10° \quad (5)$$

3.2.2 Circuit-level sizing

The architectural-level design resulted in constraints in terms of gain ($A_{preamp} > 15$), bandwidth of the preamps (e.g. $\varphi_{Nyquist} \leq \text{atan}(1/6) \approx 10°$), and admissible input-referred offset (e.g. $\sigma_{total,\,offset} \leq 0.7\ LSB$) for the different building blocks. Using these constraints, each of the building blocks can be sized as will be discussed in detail in the following paragraphs for each block: S/H, fully differential ladder, 1st stage preamplifier, 2nd stage preamplifier, comparator and digital back-end.

Sample & Hold

The S/H was based on the architecture presented in [6] using the gain-boosting technique. Three modifications were done: (1) the gate was boosted with a fixed voltage, (2) special attention was paid to the clock recovery and timing and (3) a PMOS transistor was added in parallel with the NMOS switch transistor.

The S/H was designed to steer a load of 5 pF (worst-case estimate of the total input capacitance based on mismatch constraints) with an input swing of 0.8V (the input swing is chosen by the designer and fixed during the optimization of the preprocessing chain later on). The simulated 3rd harmonic is -68dB and the 5th harmonic is -83dB at a sampling rate of 200 MS/s.

Reference ladder network

The reference ladder has to be properly sized to avoid feed-through. A first-order estimation of the feedthrough to the midpoint (worst case) of the reference ladder is given by [7]:

$$V_{mid}/V_{in} = \frac{\pi}{4} f_{in} R_{ladder} C \quad (6)$$

In this formula f_{in} is the input frequency. R_{ladder} is the total resistance in the case of one ladder. C stands for the total coupling capacitance from the input to the reference ladder (the gate-source capacitance of the input transistors of the preamplifiers). The maximum resistance R_{ladder} is calculated to be 14 Ω.

Preamplifier stage 1

The schematic of the first stage preamplifier is shown in Fig. 5. The input referred offset was calculated using ISAAC [8]:

$$\sigma^2_{preamp\_st1} = 4\left[\sigma^2_{M_1} + \left(\sigma^2_{M_{33}}/\sqrt{2}\right) + \sigma^2_{M_3} + \sigma^2_{M_4}\right] \quad (7)$$

The gain A_{preamp_st1} of this preamplifier is a function of the number of averaging nr_{AVG} and the number of interpolations nr_{INT}. In [4] a new preamplifier topology was proposed which has high impedance load, which is beneficial for averaging. The presented preamplifier exhibits the same advantage of high intrinsic impedance load (formed by transistors M_{33} and M_4). Thus the gain in the preamplifier and the averaging effect no longer have to be traded off [4].

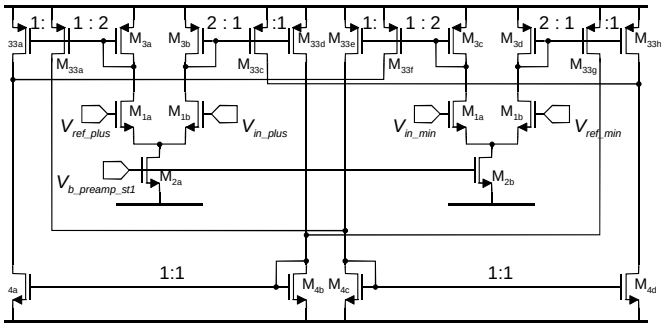

Figure 5: Schematic of the 1st stage preamplifier.

Using macro models for the amplifiers, a closed expression for the overall gain of the preamplifier as a function of the number of averaging nr_{AVG} and the number of interpolations nr_{INT}, was calculated using the ISAAC tool [8]. Fig. 6 shows the case where $nr_{AVG}=5$ and $nr_{INT}=2$. Similar macro models were used to derive equations for other values of nr_{INT} and nr_{AVG}. Comparing the different equations resulted in a closed expression for the gain:

$$A_{preamp\_st1} = -2 \cdot \frac{gm_{m1}}{g_{AVG}} \cdot \frac{nr_{INT}(nr_{AVG}+1)^2}{2^3} \quad (8)$$

This expression is a function of the amount of averaging nr_{AVG} and the number of interpolations nr_{INT}.

Not only the gain, but also the frequency behavior is affected by the averaging. Expressions were derived for the dominant pole as

a function of both the number of averaging nr_{AVG} and the number of interpolations nr_{INT} :

$$f_{dominant\_st1} = \frac{1}{2\pi \cdot f(nr_{AVG}, nr_{INT}) \cdot R_{AVG} \cdot C_{load}} \quad (9)$$

where $f(nr_{AVG}, nr_{INT})$ is a fit factor extracted from simulations. This fit factor *f(·)* is a function of both the number of averaging nr_{AVG} and the number of interpolations nr_{INT}.

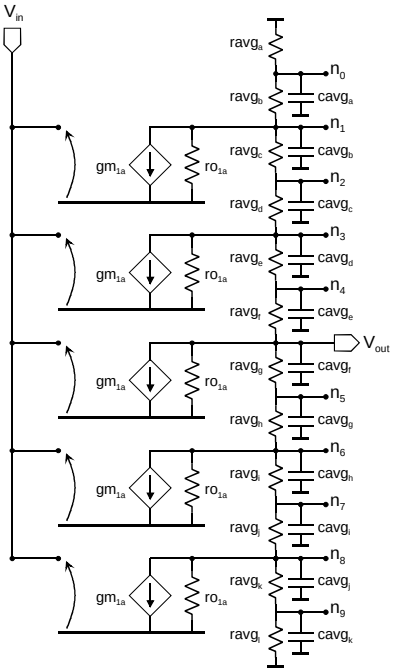

Figure 6: Simplified schematic for preamplifiers in case of nr_{AVG}=5 and nr_{INT}=2.

Preamplifier stage 2

For the second-stage preamplifier, the topology presented in [4] was used. The mismatch contribution is given by:

$$\sigma^2_{in\_st2} = \sigma^2_{m1} + 2\sigma^2_{m3}(gm_{m3}/gm_{m1})^2 \quad (10)$$

Also the 2nd stage preamplifier has a high output impedance. Equation (8) also gives the gain of the 2nd stage preamplifier but then as a function of the amount of averaging $nr_{AVG,st2}$ and the number of interpolations $nr_{INT,st2}$. The frequency behaviour was equally addressed. An equation for the dominant pole, similar to equation (9), has been derived.

Regenerative comparator

The comparator used in this A/D converter is a very fast regenerative structure, depicted in Fig. 7.

During the reset phase the regenerative nodes n_{r1} and n_{r2} are 'shorted' by the switch M_4. The reset time constant can be approximated by [9,10]:

$$\tau_{res} \cong \frac{C_{eq}}{g_{m5} + g_{m6} - g_{o5} - g_{o6} - 2g_{ds4}} \quad (11)$$

where C_{eq} is the total capacitance on the nodes n_{r1} and n_{r2}.

During the regeneration phase (clock is low) the injection of the current imbalance stops, and the conductance of the switch M_4 drops to zero. The regeneration speed is governed by a positive pole approximately given by [9,10]:

$$p_{reg} \cong \frac{g_{m5} + g_{m6} - g_{o5} - g_{o6}}{C_{eq}} \quad (12)$$

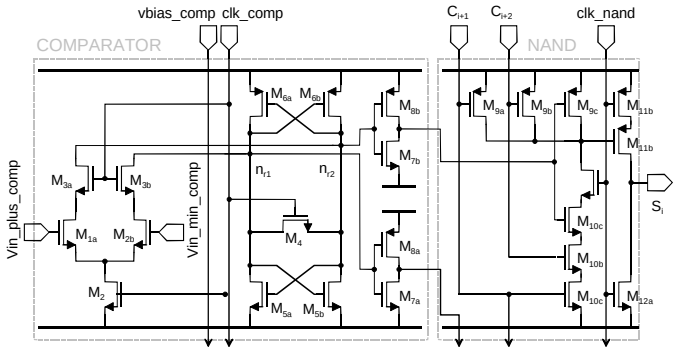

Figure 7: Schematic of the comparator & the digital back-end

Digital back-end logic

The outputs of the comparators form a thermometer code: all comparator outputs below the input level are '1' and vice versa. The thermometer code is then converted into Gray code in a ROM decoder. A flash converter with this type of structure typically suffers from two problems: bubbles in the thermometer code and metastability [10]. The simplest circuit that can detect a bubble is a 3 input and-gate to ensure only a single one drives the ROM, as shown in Fig. 7. To avoid metastability two asymmetric inverters (M_7/M_8 in Fig. 7) were inserted [10].

Sizing plan

Combining these equations with the set of constraints resulting from architectural-level synthesis, a full design plan for the converter was derived. The architectural design resulted in three constraints for the design of the preamplifier stages:

$$A_{preamp\_st1} = 10, \; A_{preamp\_st2} = 2 \quad (13a)$$

$$\varphi_{Nyquist} \le \text{atan}(1/6) \approx 10° \quad (13b)$$

$$\sigma^2_{preamp\_st1} \le \tfrac{3}{4}(0.7LSB)^2, \sigma^2_{preamp\_st2} \le \tfrac{1}{4}(0.7\,LSB)^2 \quad (13c)$$

With these constraints, and the complete set of design equations derived, all transistors can be sized. As the inter dependency of the different design variables is high, the sizing plan has been formulated in a (global) constraint optimization that has been resolved using advanced simulated annealing (ASA) where the power consumption and chip area of the circuit is minimized [11]. The phase shift constraint is evaluated using equation (4) during optimization. The offset constraint is implemented as a lookup table and checked as the amount of averaging nr_{AVG} evolves during optimization. The overdrive voltages V_{GS}-V_T of the preamplifiers, the lengths L of the transistors, the biasing currents and the averaging resistor values r_{AVG} are the input variables of the optimization. The input range was fixed during optimization as was the number of interpolations which was chosen $nr_{INT,st1}$=4 and $nr_{INT,st2}$=2.

The resulting global optimization problem is formulated as:

$$\underset{\underline{x}}{\text{minimize}}\, C(\underline{x}) = \sum_{i=1}^{k} w_i \cdot f_i(\underline{x}) + \sum_{j=1}^{l} w_j \cdot g_j(\underline{x}) \quad (14)$$

where $\underline{x}$ is the set of independent variables as listed in Table 2, $\underline{f}(\underline{x})$ is a set of k objective functions, and $\underline{g}(\underline{x})$ denotes a set of l constraints. Constraint functions are formulated such that a constraint is satisfied when $\underline{g}(\underline{x}) \le 0$.

Table 2: Input variables x_i for the 1st & 2nd stage preamplifier and comparator.

	1st stage preamp	2nd stage preamp	comparator
x_i	L_1, L_2, L_3=L_{33}, L_4	L_1, L_2, L_3	L_1, L_2, L_5, L_6, L_4, W_4
	$(V_{GS}\text{-}V_T)_{M1}$, $(V_{GS}\text{-}V_T)_{M2}$, $(V_{GS}\text{-}V_T)_{M3}$, $(V_{GS}\text{-}V_T)_{M4}$	$(V_{GS}\text{-}V_T)_{M1}$, $(V_{GS}\text{-}V_T)_{M2}$, $(V_{GS}\text{-}V_T)_{M3}$	$(V_{GS}\text{-}V_T)_{M1}$, $(V_{GS}\text{-}V_T)_{M2}$, V_{reset}
	$I_{DS,2}$	$I_{DS,2}$	$I_{DS,2}$, $I_{DS,5}$
	$R_{AVG,st1}$, $L_{AVG,st1}$,, $nr_{AVG,st1}$	$R_{AVG,st2}$, $L_{AVG,st2}$,, $nr_{AVG,st2}$	

The cost function is built by a weighted sum of functions that force the optimization to evolve to *operational* (saturation/linear region), *functional* (design requirements fulfilled) and *applicable solutions* (specifications met). Within this last design subspace, trade-offs are optimized to result in a solution with minimal area and power. These four categories of cost terms have weighting terms which typically differ an order of magnitude in order to guide the optimization.

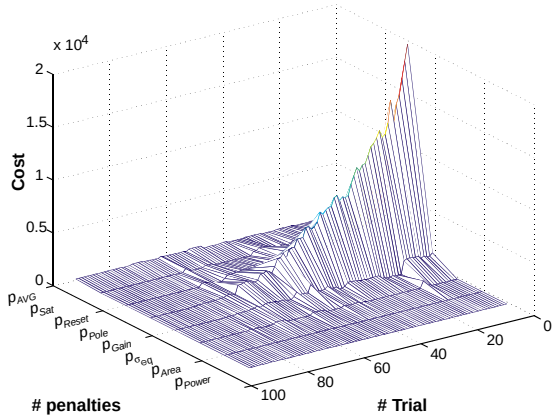

Figure 8: Global cost during sizing using ASA.

For the MOS transistors the input set is chosen to be:

$$\underline{x}_{Mi} = \{L, V_{GS} - V_T, I_{DS}\} \qquad (15)$$

A level-1 Spice model was encapsulated in a separate Matlab routine. Given L, $V_{GS} - V_T$ and I_{DS}, the routine returns W, g_m, g_o, σ and the parasitic C_{GS}, C_{GD}. Other device-level evaluations (e.g. BSIM) could be used as well, by either a Matlab routine or an external C-code routine which can be invoked easily form within the Matlab environment.

For designing the averaging resistors, an additional routine was added in Matlab. The routine takes the resistive value R_{AVG} and the length L_{AVG} as inputs and decides in which layer to implement the resistor (e.g high-resistive poly, low-resistive poly) such as to minimize parasitic capacitance. The routine returns the width W_{AVG} and the parasitic capacitance C_{AVG}.

The amount of averaging nr_{AVG} is needed to calculate the averaging effect and thus the constraint on the admissible input-referred offset $\sigma_{total,offset}$. The amount of averaging nr_{AVG} is however not an independent variable, and is calculated from the V_{GS}-V_T, the gain and the linear output range of the preamplifier stages. This loop is resolved by choosing $nr_{AVG,st1}$ and $nr_{AVG,st2}$ as input variables and forcing them to be equal to the actual nr_{AVG} calculated.

The simulated annealing loop was implemented in the Matlab environment and uses the Advanced Simulated Annealing (ASA) C-routine as actual algorithm [11]. The evolution of the total cost term during sizing is depicted in Fig. 8. About 30 trials were needed to obtain the final result. One trial takes 14 min on a Sunblade 1000 workstation.

The sizing of the S/H, the reference ladder network and the digital back-end was not included in the global optimization. The S/H was designed using ELDO in the loop, while the digital back-end was designed manually.

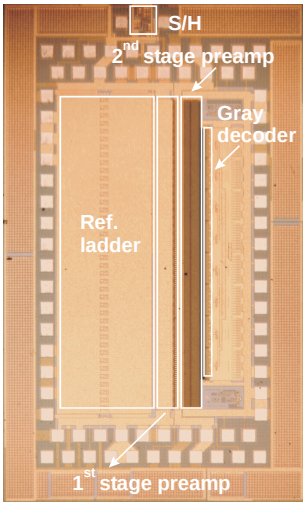

Figure 9: Micro photograph of the A/D converter.

3.2.3 *Layout*

The floorplan follows directly from the block diagram in Fig. 2; the result is depicted in Fig. 9. Around the perimeter of the chip 1 nF of decoupling capacitance has been integrated to provide stable power supplies.

The reference ladder was implemented in metal-1 layer. Dummies were added to provide identical surroundings. An additional decoupling capacitance of 10x30pF was added to each ladder to provide stable reference levels.

The layout of the preamplifiers and the routing was done manually: devices were generated using LAYLA [12], placement of the different modules (1st & 2nd stage preamplifier) was done using MONDRIAAN [13]. Internally an additional 500 pF of decoupling capacitance was added. Guard rings were used to reduce substrate (digital) noise coupling.

The layout of the digital back-end was done combining Virtuoso from Cadence and the MONDRIAAN tool [13]. The layout of the comparator was done manually as was the internal routing, transistors were generated using the LAYLA tool. The ROM cell is handcrafted, 8 ROM cell constitute a ROM line. MONDRIAAN is used to place the ROM cell and connect the cells using a listing of the Gray code as input. The ROM is generated within 1 minute.

The clock distribution is critical for analog design, and available digital tools cannot deal with the specific analog requirements. A buffered binary clock tree takes care of equal delay, which would otherwise deteriorate the dynamic performance. The design and layout of this clock buffer was done manually.

3.3 Verification Phase

After sizing the design was verified with device level simulations using ELDO. Layout parasitics are extracted and the static performance was verified with Monte-Carlo simulations considering process variations using the in-house developed tool MIMI [14]: a mismatch offset voltage and offset current are automatically added to the netlist.

The offset of the comparator was automatically extracted with an in-house developed tool presented in [1]. The offset is determined by narrowing down the input voltage interval for which the comparator toggles. A regeneration time constant τ_{reg} of 50 ps was simulated.

4. MEASUREMENTS

The A/D converter was processed in a 0.35µm CMOS process. The A/D converter was mounted on a ceramic substrate; all biasing was generated on the substrate to minimize incoupling noise. The analog power preprocessing chain runs from a 3.3 V power supply, the digital back-end runs at 2.5 V. All measurements were done at full speed of 200 MS/s [3]. The analog preprocessing chain consumes 285 mW, the reference ladder consumes 250 mW and the digital part consumes 120 mW worst case.

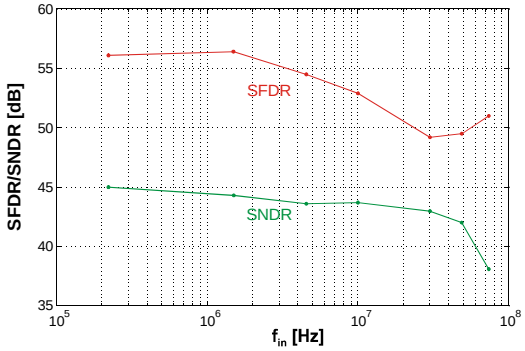

Figure 10: Measured dynamic performance: SFDR>50 dB and SNDR > 43 dB.

Static performance measurements show an INL < 0.95 LSB and a DNL < 0.8 LSB. The dynamic performance is shown in Fig. 10. A Signal-to-Noise-and-Distortion-Ratio (SNDR) of 44.3 dB is achieved at low frequencies; at 30 MHz a SNDR figure of 43 dB was measured.

5. CONCLUSIONS

The systematic design of an 8-bit interpolating/averaging 200 MS/s Nyquist-rate A/D converter has been presented. Using behavioral models the system specifications are translated in offset and phase shift constraints that steer the global optimization at the circuit level. The chip was processed in a standard 0.35 µm CMOS process. Measurements on the processed chip (see Table 3) yielded good results proving the viability off the presented approach.

Table 3: Specification list for a (interpolating/ averaging) A/D converter with target values and measured values.

	Specification	Unit	Target	Measured
Static	Resolution *N*	#bits	8	8
	INL / DNL	LSB	<1 / <½	0.8 / 0.9
	Yield	%	99.9	-
Dynamic	SFDR	dB	> 45	59.2
	SNDR	dB	> 40	44.3dB@1.5MHz 42.7dB@40MHz
	Sample freq.	MS/s	200	200
Environmental	Conversion rate	-	1 code/ clock cycle	1 code/ clock cycle
	Input capacitance	pF	< 5	4.8
	Input range	V_{ptp}	> 0.5	1.3 V
	Power supply	V	3.3	3.3/2.5
	Coding	-	Gray code	Gray code
Optimization	Power	mW	min	655
	Area	μm^2	min	1400x2400

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