Leakage Current Cancellation Technique for Low Power Switched-Capacitor Circuits

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ABSTRACT
In this paper, we describe a circuit technique to implement low power switched-capacitor circuits for low frequency operation. Low power consumption is crucial for medical implant devices. Reducing supply voltage is well known to minimize power dissipation. To facilitate low voltage operations, the transistor's Vth are becoming lower and lower. Low Vth transistors have high leakage currents which impact the performance of switched-capacitor circuits, sample-and-hold amplifiers and many more. A new circuit technique is presented here to largely minimize the effective leakage current when the CMOS switch is turned off. It employs an active feedback loop to automatically cancel both junction and sub-threshold channel leakage. By reducing the effective leakage current, the capacitors used in the circuit can be significantly reduced, hence lowering the overall power consumption. This is a general technique and can be used in various circuit applications

Keywords
Low power, analog, leakage current, switched-capacitor circuit, sample and hold, amplifier.

1. INTRODUCTION
Battery powered implantable medical devices and other portable devices require many years of continuous operation. Low power consumption is the most important criteria in designing the IC[1]. It is very well known that reducing the supply voltage is one of the most effective ways to reduce power consumption[2][3]. Lowering the operating voltage puts harder constraints on the analog circuits, as lower voltages are available to drive the transistor. Low Vth processes have been developed to target low voltage operations[4][5]. In addition, as devices shrink in the deep sub-micron processes, transistors are also expected to operate in low supply voltages in order to provide long term reliability. The drawback of these low Vth or sub-micron processes is that they significantly increase the leakage current. As a result, there is a residual current flow when the transistor is turned off, which has a very significant impact on switched-capacitor type of analog circuits.

This paper will first address the common problem seen in switched-capacitor circuits due to the effect of transistor leakage current. A new concept that can significantly minimize the effective leakage current to regain circuit performance will be presented, followed by a circuit implementation. The proposed technique achieves both minimal silicon area and low power operation. Finally, the measured performance and comparison is discussed.

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2. CMOS SWITCH LEAKAGE
The effect of the transistor leakage current in analog switched-capacitor types of circuit is best illustrated by an example. Consider a basic sample and hold amplifier (SHA), as shown in Figure 1.

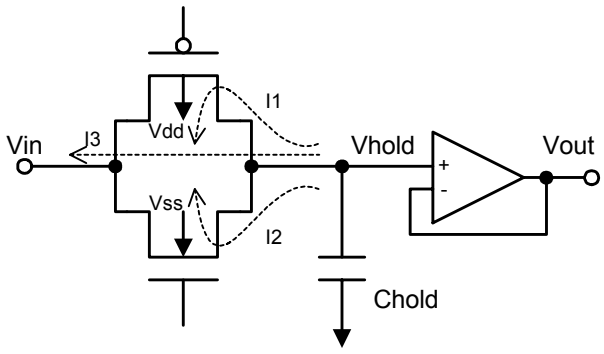

Figure 1. A basic SHA using a CMOS switch and a hold capacitor

In many medical applications, the input signals (such as cardiac rhythm sensing or neuro-responses from the body) may have a relatively low frequency spectrum, often, a corner frequency as low as ~0.1Hz is expected. Therefore SHA circuits, switched-capacitor filters or amplifiers must be able to handle hundreds of ms of hold time. In a standard sub-micron CMOS process, the leakage current of a minimum size transistor is in the order of pA,

and may be much higher for a low Vth deep sub-micron process. If a 1pF holding capacitor is used with a holding period of 100ms, then 1pA of leakage will cause a 0.1V drift at the end of the holding period. This is unacceptable in applications where mV or μV of sensitivity is required. A typical solution to overcome this problem is to use a much larger capacitor (say 10-30pF). However, a larger capacitor requires a much stronger driver or amplifier at the previous stage thus more supply current is needed. A larger capacitor also increases silicon area significantly.

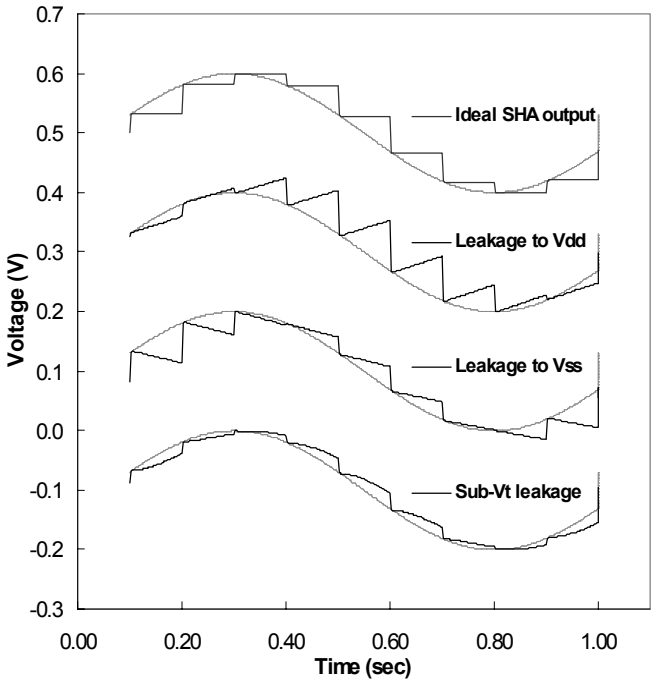

Figure 2. Example SHA outputs with various leakage

There are two main types of leakage currents from a MOS transistor: (a) the drain/source to body junction leakage and (b) the sub-Vth drain to source channel leakage. In the previous SHA example, three leakage paths are shown in Figure 1. Current *I1* is the junction leakage to Vdd, *I2* is the junction leakage to Vss, and *I3* is the channel leakage. The total effective leakage current seen by the holding capacitor is the sum of all three. Figure 2 shows some example waveforms from the SHA. A sinewave is used as an input. The first waveform is an ideal sample and hold output. The second waveform is an example of *I1* being the dominant leakage current, where the output drifts to Vdd during the hold period. The third or fourth waveforms are expected if leakage *I2* or *I3* are being dominant, respectively. These output drifts may also cause harmonic distortions. This SHA example is just one of the many switched-capacitor type of circuits which can be affected by a transistor's leakage.

3. LEAKAGE CURRENT CANCELLATION TECHNIQUE

3.1 Circuit Concept

A new technique is presented here to significantly reduce the effective leakage current[6]. Again, the previous sample and hold amplifier circuit is used for illustrating the technique. Figure 3 shows the concept of this technique. Basically, a self-adjusted current source is introduced to the system. When the CMOS switch is turned off, a compensating current, *Icancel*, is injected to the high impedance node, *Vhold*. This current is automatically adjusted such that it is equal to the sum of *I1*, *I2* and *I3*, but in the opposite direction. As a result, all leakage currents cancel out. The effective leakage seen by the hold capacitor is virtually zero. In this way, the hold capacitor, *Chold*, can be kept very small without having the voltage drift away. Therefore, the driver or amplifier at the previous stage can be kept very small and minimum supply current is needed. Hence this technique allows low power operation and requires minimal silicon area at the same time.

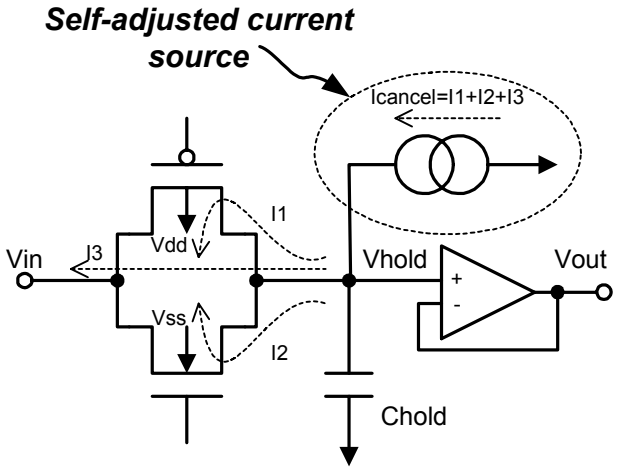

Figure 3. The concept of the leakage current cancellation technique

3.2 Design Implementation

The challenge of the proposed concept is the ability to automatically generate an accurate canceling current, *Icancel*, at any given operating voltages. One possible implementation of the above concept to the SHA is shown in Figure 4, where a replica CMOS switch network and a current cancellation feedback network are introduced.

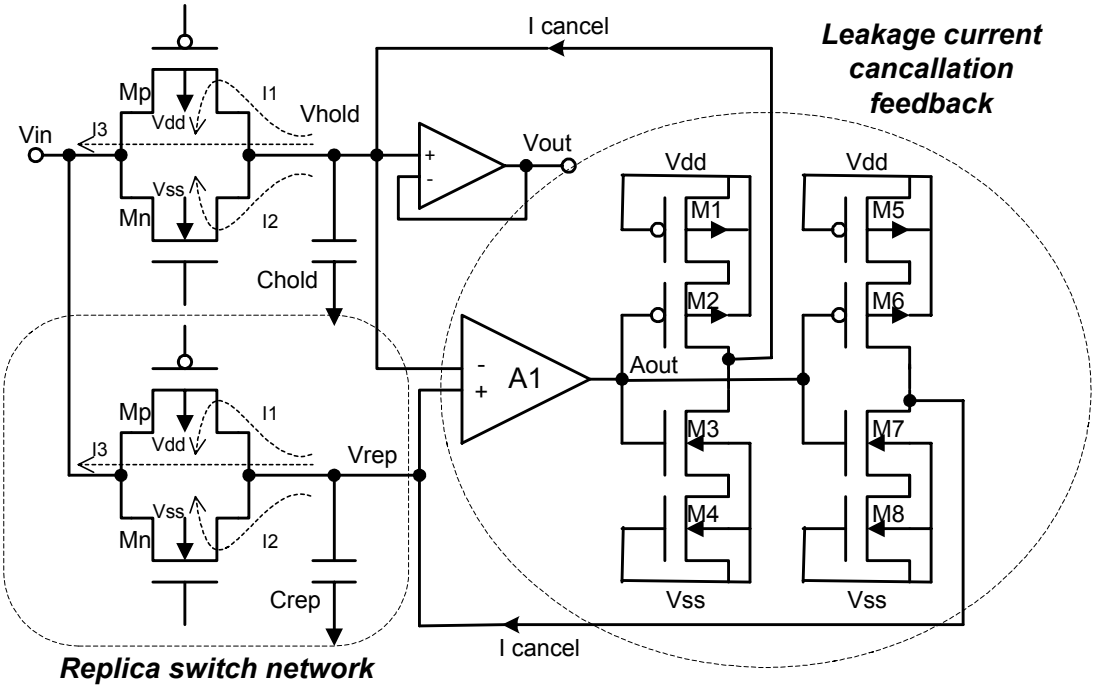

Figure 4. An implementation of the leakage cancellation technique for the SHA

In this implementation, the replica CMOS switch is identical to the main switch, whereas the replica capacitor *Crep* is much smaller than the main capacitor *Chold*. For the purpose of explanation, assume the current cancellation feedback circuit (transistor *M1-M8* and opamp *A1*) is omitted from the system. Under this configuration, all leakage currents (*I1, I2, I3*) on the main switch network are the same as the replica network, since the transistors operate under the same voltage conditions. The voltage drift on the replica node *Vrep* is much larger than the main mode *Vhold*, because *Crep* is smaller than *Chold*. Figure 5 shows the example waveforms for *Vhold* and *Vrep*, without the self-adjusted feedback network. As long as leakage currents exist from the switches, a voltage difference is expected on *Vrep* and *Vhold* when the switch is turned off.

Now, add the current cancellation feedback circuit back to the complete system and to close the loop, as shown in Figure 4. Transistors *M1, M4, M5* and *M8* are the "leakage transistors", they all have zero gate-source voltage. Their dimensions are much larger than the sample-and-hold CMOS switches: *Mp* and *Mn*. These "leakage transistors" can be viewed as constant current sources, and their currents are higher than the *Mp* and *Mn* leakages. By utilizing an operational amplifier, *A1,* and a push-pull output stage with the "leakage transistors", a closed loop system is formed. The closed loop system monitors the voltage difference between *Vhold* and *Vrep* continuously, then injects the counter-current, *Icancel*, to cancel the CMOS switch leakages accordingly. The system will reach a quiescent mode at which *Icancel* is equal to the CMOS switch leakage, and both *Vhold* and *Vrep* will not drift any further. Both transistor junction and channel leakages from the CMOS switch are taken into consideration and are able to be cancelled by the proposed feedback network.

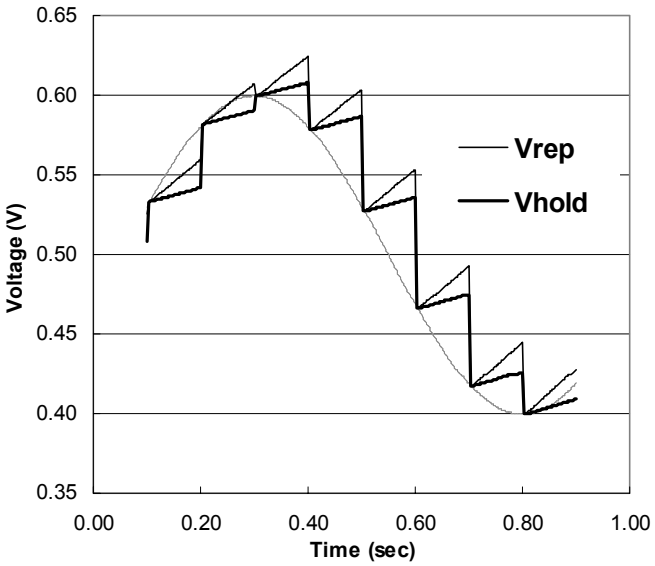

Figure 5. Example waveforms of *Vhold* and *Vrep*, without the self-adjusted current feedback network

Theoretically, if the operational amplifier *A1* is ideal (infinite voltage gain, zero input offset voltage) and all transistors are perfectly matched, then all the CMOS switch leakage currents will

be perfectly canceled out. The effective leakage current seen by the capacitors will be absolutely zero. However, transistors can never be matched perfectly on real silicon. The operational amplifier will always have finite gain and offset errors. The voltage difference between *Vhold* and *Vrep* under the closed-loop quiescent mode can be expressed as

$$Vdiff = Vhold - Vrep = \frac{Aout}{A} + V_{offset} \quad (1)$$

where A is the operational amplifier gain and V_{offset} is the input offset voltage.

This voltage difference will lead to a leakage current mismatch between the main and replica switches. The voltage drift on the node *Vhold* in this closed loop system can be expressed as:

$$\frac{dV_{hold}}{dt} = \frac{I_{delta}}{Chold - Crep} \quad (2)$$

where I_{delta} is the current mismatch between the main and replica switches, and it is a function of *Vdiff:*

$$I_{delta} = f(Vdiff) = f(\frac{Aout}{A} + V_{offset}) \quad (3)$$

From equation (2), the voltage drift on *Vhold* depends on leakage current mismatches and capacitor sizes. To minimize the voltage drift, *Idelta* should be as small as possible, whereas *Chold-Crep* should be as large as possible. *Idelta* can be minimized by performing careful layouts and having a high open loop gain operational amplifier. To maximize the term *Chold-Crep* while having minimal power consumption, *Crep* should keep very small. However, if *Crep* is too small, the clock injection from the CMOS switch can be severe which introduces offset errors during the holding period. Therefore, there is an optimum *Crep* and *Chold* value for every application.

3.3 Simulations

The proposed leakage cancellation SHA circuit shown in Figure 4 has been designed and simulated. Figure 6 shows the simulated waveforms, with *Chold*=0.5pF and *Crep*=0.1pF. Operational amplifier, *A1*, is a single stage design, which consumes only a few nA. The voltage drift during hold mode is 9.5mV/sec, whereas the uncompensated circuit has 200mV/sec drift. More than 20x of improvement is observed by using the proposed technique.

Table 1 shows the performance comparison between three different SHA circuit implementations. The first approach being the uncompensated SHA circuit as shown in Figure 1, which has an unacceptable amount of voltage drift. The second approach is a compensated circuit with a large holding capacitor to meet the voltage drift requirement. The third approach is the proposed leakage cancellation technique shown in Figure 4.

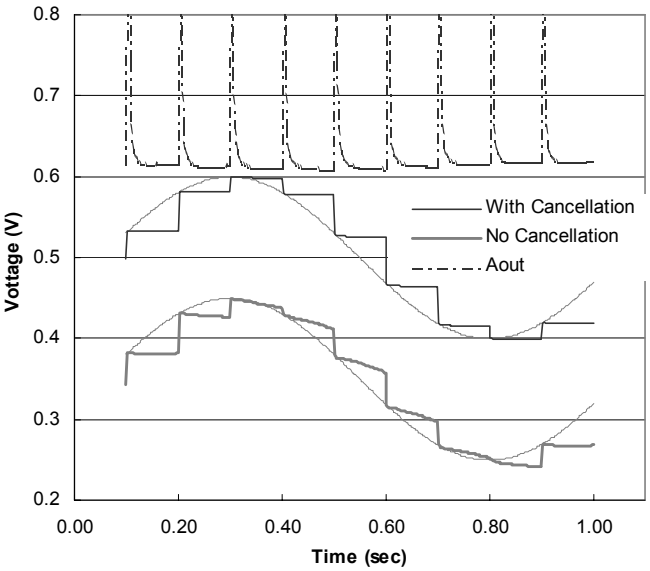

Figure 6. Output waveforms with and without the leakage cancellation technique

Table 1. Performance comparison between different SHA approaches

Approach	Silicon Area	Power	Adv/Disadv
Uncompensated SHA	~2,500μm^2	~30nA	Unacceptable drift
Compensated with a larger capacitor	~20,000μm^2	~200nA	High power, Large area
Proposed leakage-cancel technique	~5,700μm^2	~38nA	Low power, Small area

4. MEASURED PERFORMANCE

The SHA described above is one of the many possible applications where the proposed technique can be used. This leakage cancellation technique can be applied to many different circuits that involve switches and capacitors. A first-order switched-capacitor low-pass filter was implemented on a test chip amongst other analog circuits. It was fabricated in a CMOS 2-poly 3-metal 0.5μm technology. Figure 7 shows the input, output, and clocking waveforms of an uncompensated circuit. Figure 8 shows the waveforms of the leakage-cancellation circuit using the proposed idea.

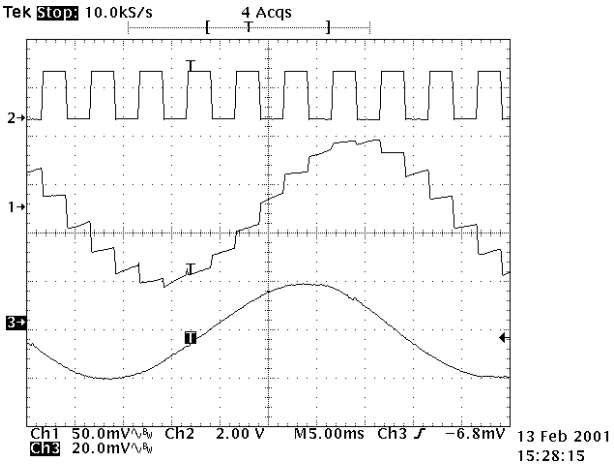

Figure 7. Waveforms from the uncompensated SHA circuit

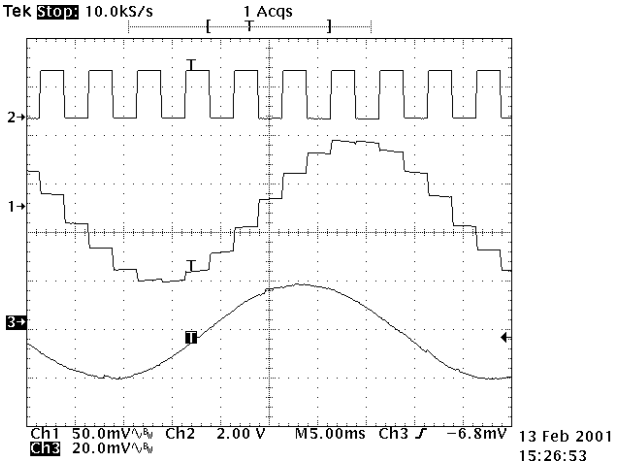

Figure 8. Waveforms from the leakage-cancellation circuit

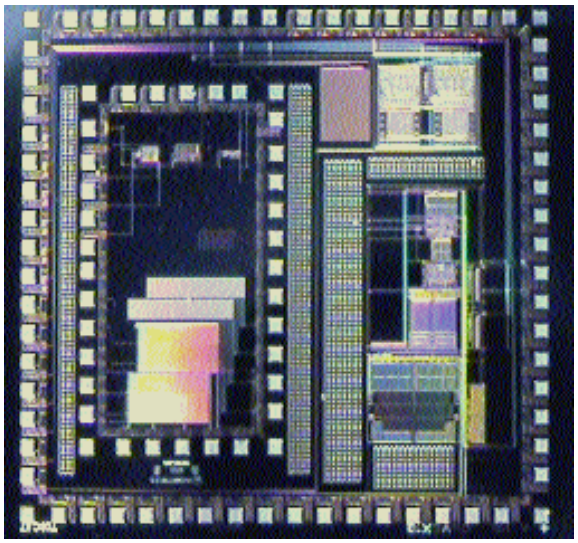

Figure 11. Die photo of the test chip

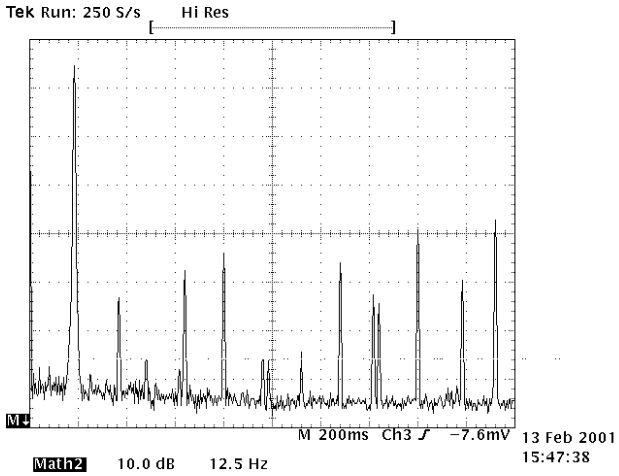

Figure 9. FFT of the uncompensated SHA circuit

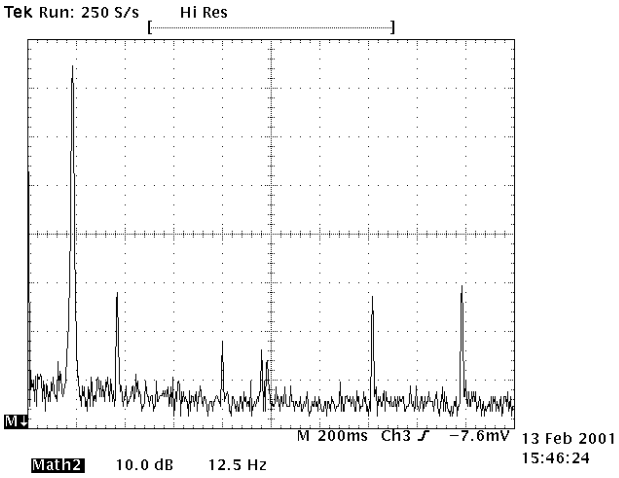

Figure 10. FFT of the leakage-cancellation circuit

Figure 9 shows the frequency spectrum of the uncompensated circuit. The SNR of the output is ~30dB. The frequency spectrum from the leakage-cancellation circuit is shown in Figure 10, the SNR is ~45dB. A 15dB SNR improvement is seen using the proposed technique. Figure 11 shows the die photo of the chip.

5. CONCLUSION

A leakage current compensation technique for low power switched-capacitor circuits has been presented. It largely reduces the effective leakage current, whereby smaller capacitors can be used in the circuit, to achieve low power operation and small silicon area at the same time. A significant improvement is seen on power consumption, silicon area and circuit performance. It is a general technique that can be applied to many different applications. Simulation and measurement results have also been shown.

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