Multi-Hit Time-to-Digital Converter VLSI for High-Energy Physics Experiments

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Abstract— A multi-hit time-to-digital converter VLSI has been developed using a CMOS 0.3 μm gate-array technology. The chip is designed for use in a high-energy physics experiment ATLAS. Precise timing signals are generated from 16 taps of an asymmetric ring oscillator oscillating at 80MHz and controlled by a PLL circuit. A prototype chip has been developed, and a time resolution of 300 ps RMS was obtained. Many macro cells are developed to achieve such high resolution still using commercial gate-array technology.

1. INTRODUCTION

World largest proton-proton colliding-beam accelerator LHC (Large Hadron Collider) is now under construction at CERN (European Organization for Nuclear Research) in Geneva. One of the experiments at the LHC is ATLAS experiment [1] which will start to run on July 2005.

Muon detector of the ATLAS requires a high-rate (~400 kHz) time-to-digital converter (TDC) with a sub-nano second time resolution. The TDC receives detector signal and measures the time of the leading edge and its pulse width. The measured data must be kept in the chip until a trigger signal issued about 3 μsec later.

Since the number of channels used are very large (370k channels), the device must be low power, high density and low cost. In addition, the chip will be attached to the detector, so it must have adequate radiation tolerance for gamma-rays, neutrons and charged particles.

We have developed several kinds of TDC LSI's called a time memory cell (TMC) [2], but the new TDC (named AMT: ATLAS Muon TDC) is more demanding [3]. In addition to the time digitizer circuit, it also includes data processing unit which selects relevant data to a trigger, LVDS input/output, a JTAG interface, and a Built-In Self-Test circuit for memories. The chip was developed by using a 0.3 μm CMOS gate-array technology (Toshiba TC220G). The number of used gate is about 110 k gates.

Although the technology is a gate-array, we have made intensive analog simulation and paid much attention to cell layout to achieve a sub-nano second timing resolution. Several macro cells are developed for time critical and analog parts. Careful floor planning are done to minimize route of the time critical signals.

Here we report about a prototype chip, called AMT-1, which has full functionality for the experiment. After system tests with detectors the chip will be massively produced.

1. CIRCUIT DESCRIPTION

Photograph of the AMT-1 chip is shown in Fig. 1 and its block diagram is shown in Fig. 2.

Accurate timing signals are derived from an asymmetric ring oscillator [4] (Fig. 3) which is stabilized with a Phase Locked Loop (PLL) circuit. The PLL locks at 80 MHz from a LHC beam clock (40MHz). By dividing the 12.5 ns clock period into 16 intervals a time bin size of 0.78 ns is obtained (fine time). To extend timing range, there is a 13 bit counter which is counted up at 80 MHz (coarse time).

Although normal ring oscillator has odd number of stages, the asymmetric oscillator can generate even number of equally separated timing signals. This feature is very desirable to get a binary number by combining the fine time and the coarse time. Furthermore each stage of the oscillator is very simple and well fit to the gate-array structure (2 PMOS and 2 NMOS transistors) while attaining adequate timing resolution.

When a hit signal is arrived, the fine time and the coarse time are stored in individual channel buffers. The time of both leading and trailing edge of the hit signal can be stored. Each channel has a 4-word buffer where measurements are stored until they can be written into the common level 1 buffer. In a pulse width measurement mode, the width is calculated before storing to the level 1 buffer.

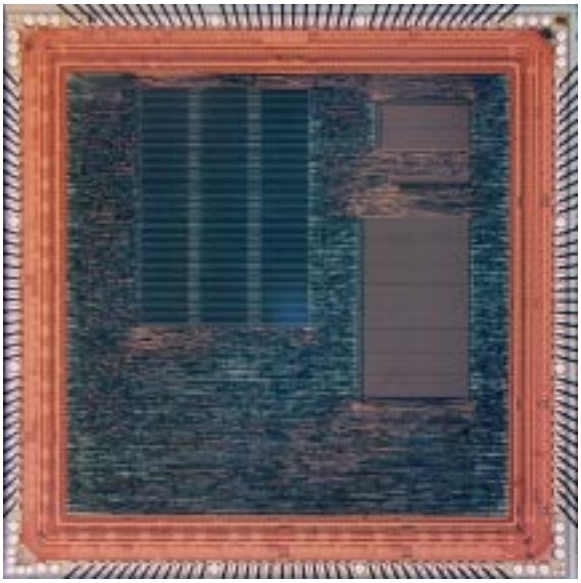

Fig. 1 Photograph of the AMT-1 chip. The die size is about 6 mm by 6 mm.

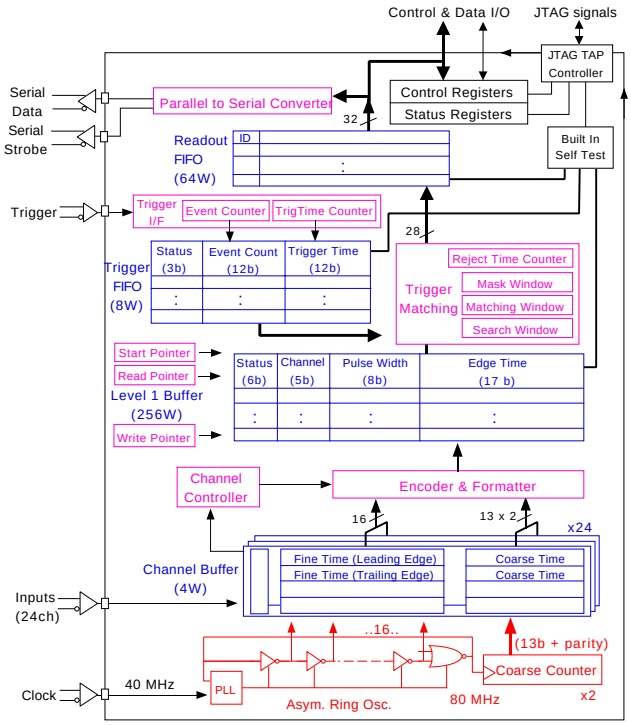

Fig. 2 Block diagram of the AMT-1 chip.

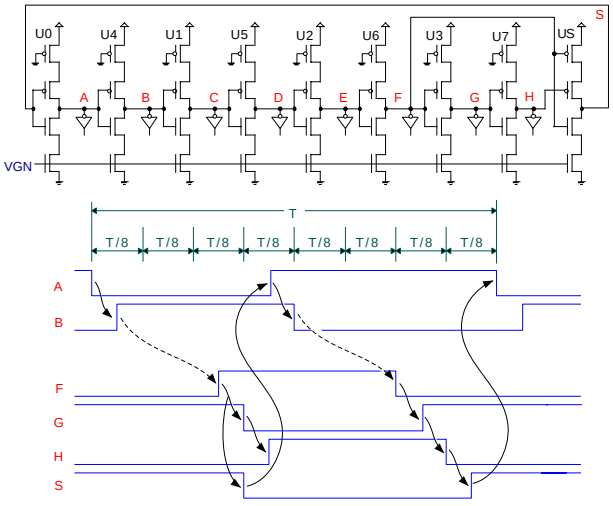

Fig. 3 Eight stages asymmetric ring oscillator. In AMT-1 16 stages are used. VGN is a delay control signal from the PLL. Falling edge timings of nodes A~H are used.

2. Measurement Results

A. *PLL and Ring Oscillator*

We observed the jitter of the PLL circuit by measuring the time distribution of the oscillator output relative to an input clock. Standard deviation of the distributions for different frequencies and power supply voltages are plotted in Fig. 4. The jitter is about 140 ps at operating condition (80 MHz and 3.3V) and the PLL is stable in broad range (20-140 MHz, 2.9-3.7 V). This value is small enough for our purpose which requires sub-nano second resolution.

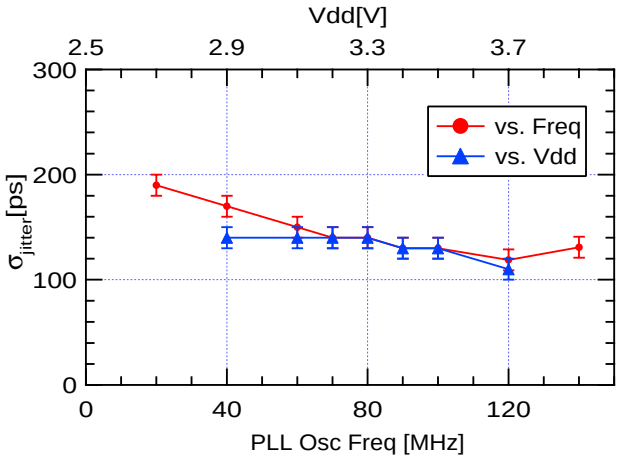

Fig. 4 PLL jitter measurement. Distributions of the jitter are measured, and their standard deviations are plotted for each oscillating frequency and supply voltage (Vdd).

B. *Time Resolution and Non-Linearity*

Time resolution was measured by supplying a clock synchronous hit signal to the input and varying the delay time of the signal. The RMS (root mean square) value of 300 ps, which includes quantization error of 225ps, is obtained.

Non-linearity of the time measurement was also measured by applying a hit signal for which the delay time is uniformly distributed, and counting the number of hits recorded in each bin. Both the Differential Non-Linearity (DNL) and Integral Non-Linearity (INL) are small enough (RMS < 70 ps) for our purpose.

3. Summary

A prototype TDC chip (AMT-1) was developed for high-energy physics experiments. The chip was fully functional and 300ps RMS resolution was obtained. Total power consumption of the chip is around 500 mW. Most power consuming parts in present design is LVDS receivers (30 receivers). Reduction of the power is planned by optimizing the receiver circuit. Mass production is scheduled at the end of year 2001.

Acknowledgements

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Reference

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[4] "Voltage-Controlled Oscillating Circuit", Japanese patent No. 2663397, US patent No. 08/380,580, European Patent No. 95300652.5