How to Efficiently Capture On-Chip Inductance Effects: Introducing a New Circuit Element K

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Abstract

On-chip inductance extraction and analysis is becoming increasing critical. Inductance extraction can be difficult, cumbersome and impractical on large designs as inductance depends on the current return path — which is typically unknown prior to extracting and simulating the circuit model. In this paper, we propose a new circuit element, K, to model inductance effects, at the same time being easier to extract and analyze. K is defined as inverse of partial inductance matrix L, and has locality and sparsity normally associated with a capacitance matrix. We propose to capture inductance effects by directly extracting and simulating K, instead of partial inductance, leading to much more efficient procedure which is amenable to full chip extraction. This proposed approach has been verified through several simulation results.

1 Introduction

Increasing clock speeds, die sizes, and power dissipations have driven VLSI manufacturers to abandon the simple scaling approach of interconnect wiring. Instead, they employ a hierarchy of metal wiring levels. Thinner wiring levels are used at the circuit level where density is required, and thicker layers at the top or global levels in order to route low-skew clock trees, low-loss power distribution buses, and the fastest signal interconnects. This trend, coupled with the recent introduction of copper wiring (because its resistivity is approximately half that of aluminum wiring) has made on-chip inductance modeling necessary for clocks and the fastest signal interconnects.

Inductance extraction is difficult because mutual inductance depends on the current return path — which is unknown prior to extracting and simulating a circuit model. Rosa introduced the concept of partial inductances to avoid this difficulty by assuming that each segment has a return current at infinity [2]. Ruehli introduced partial inductance to modern ICs and proposed the PEEC (Partial Equivalent Element Circuits) model to handle general three dimensional interconnects [3, 4]. Kamon, *et al* more recently developed the algorithm, FastHenry [5], to solve for effective inductance from partial inductances with multi-pole acceleration.

Nonetheless, the partial inductance approach, which assigns portions of the loop inductances to segments along the loop, results in a large, densely-coupled network representation, which makes subsequent circuit simulation practical only for small examples. Moreover, unlike capacitance matrices which can be truncated to represent only localized couplings, simply discarding distant mutual inductances can result in an unstable equivalent circuit model (positive poles) [6].

As an alternative to simple truncation, a shift-truncate potential method was proposed by Krauter, *et al* [7, 6]. This shift-truncate potential method assumes that segment currents return at a finite radius r_0, instead of infinity. Therefore, segments spaced more than r_0 apart have no inductive coupling. This technique can guarantee to generate positive definite sparse approximations of the original partial inductance matrix. Nevertheless, to determine a proper value of r_0 to ensure a desired accuracy involves complicated schemes and iterations. Moreover, this approach does not work well for long wires. Shepard, *et al* proposed the concept of "return-limited loop inductance" to sparsify the partial inductance matrix [8]. It is based on the assumption that the currents of signal lines return within the region enclosed by the nearest same-direction power-ground lines. However, this may not be true when power-ground lines are of same order of dimensions as signal lines. Recently, Lin developed the 2x mutual inductance screening rule [9]. Since this rule basically discards the consideration of circuit topology, it cannot be applied to some complex interconnect topology, such as mesh ground plane [6].

Thus, unlike capacitance extraction, where only the nearest neighbor conductors need to be considered, in inductance extraction, a large number of conductors are involved. Techniques used in capacitance extraction, such as library construction and analytical formulas cannot be applied to inductance extraction.

However, although C matrix is sparse, the inverse of C has been observed to be dense. We speculated that if L is dense, then the inverse of L may be sparse. In this paper, we introduce a new circuit element to represent inductance

effect, while still preserve locality for large systems. This new circuit element, K, is basically the inverse of partial inductance.

Therefore, we proposed to capture on-chip inductance effect by directly extracting and simulating K, instead of partial inductance. Since K has locality, we only need to consider a small number of neighbors. As the result, the K matrix for circuit simulation is very sparse. Thus it can save a great amount of CPU time and memory usage when capturing on-chip inductance effect. Moreover, we can further construct libraries or analytical formulas for K, which will enable this K-based method to be a practical one to predict and capture inductance effect for the whole chip. This new concept has been verified by the simulation results of practical examples.

2 Partial Inductance

Since our proposed K is defined as the inverse of the partial inductance, we begin with a brief review of partial inductance.

It's well known that inductance is a property of closed loops. Since for on-chip interconnects, the induced current return paths are unknown, the prevailing inductance models are built on partial inductance concepts. Partial inductance are best understood in terms of the normalized magnetic vector potential drop along a conductor segment due to current in that, or another segment. Consider the two conductor segments, i and j, as shown in Fig. 1.
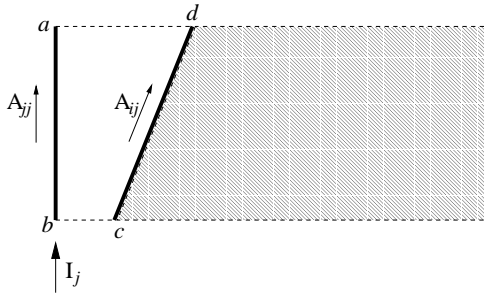

Figure 1: Partial inductance associated with magnetic vector potential drop along the conductor segments. Both segment loops are assumed to close at infinity.

The partial inductance L_{ij} between segment i and j is given by

$$L_{ij} = \frac{\frac{1}{a_i}\left[\int_{a_i}\int_{l_j}\mathbf{A}_{ij}\cdot d\mathbf{l}_i\, da_i\right]}{I_j} \quad (1)$$

where A_{ij} is the magnetic vector potential along segment i due to the current I_j in segment j. Segment i has a cross section a_j. In magneto-statics, the relationship between the magnetic vector potential A_{ij} and the current I_j is given by

$$A_{ij} = \frac{\mu_0}{4\pi a_j}\left[\int_{a_j}\int_{l_j}\frac{\mathbf{I}_j}{r_{ij}}\, d\mathbf{l}_j\, da_j\right] \quad (2)$$

where r_{ij} is the geometric distance between two points in segment i and j.

Substitute Eq. (2) into Eq. (1), we can get

$$L_{ij} = \frac{\mu_0}{4\pi a_i a_j}\left[\int_{a_i}\int_{a_j}\int_{l_i}\int_{l_j}\frac{d\mathbf{l}_i\cdot d\mathbf{l}_j}{r_{ij}}\, da_i\, da_j\right] \quad (3)$$

The partial inductance matrix for a set of n conductors is an $n \times n$ real symmetric matrix. The corresponding linear system is given by

$$\begin{bmatrix} L_{11} & L_{12} & \cdots \\ L_{21} & L_{22} & \cdots \\ \vdots & \vdots & L_{nn} \end{bmatrix}\begin{bmatrix} I_1 \\ \vdots \\ I_n \end{bmatrix} = \begin{bmatrix} \sum_{i=1}^{n}\left(\frac{1}{a_1}\int \mathbf{A}_{1i}\cdot d\mathbf{l}_1 da_1\right) \\ \vdots \\ \sum_{i=1}^{n}\left(\frac{1}{a_n}\int \mathbf{A}_{ni}\cdot d\mathbf{l}_n da_n\right) \end{bmatrix} \quad (4)$$

From Eq. (3), we can see that the partial inductance L_{ij} only depends on the relative position and length of segment i and j, and is independent of the existence of other conductors. That is to say, the existence of other conductors has no shielding effect on the inductive coupling between segment i and j, under this partial inductance definition. Furthermore, since the integral kernel of L_{ij} is r_{ij}, the off-diagonal elements in the partial inductance matrix decrease very slowly (at the order of $\log r_{ij}$) with the increase of spacing r_{ij}. Because of this long range inductive coupling effect for partial inductance of on-chip wires, capturing inductive couplings becomes much more difficult than capturing capacitive couplings, which is known to be local. Moreover, it is understood that making the matrix sparse by merely discarding the smallest terms can render the matrix indefinite and thereby introduce positive pole(s) in subsequent circuit simulations.

3 Circuit Element K

3.1 Definition of K

$[K]$ is defined as inverse of partial inductance matrix $[L]$.

$$[K] = [L]^{-1} \quad (5)$$

This definition originated from the well known relationship between capacitance and inductance for transmission line structures,

$$[L_{loop}] = \mu_0 \epsilon_0 [C_0]^{-1} \quad (6)$$

where ϵ_0 and μ_0 are permittivity and permeability in free space, respectively. $[C_0]$ is the capacitance matrix which would result if all dielectric layers were replaced by free space. This relationship inspired us that for structures other

than transmission lines, although the inverted inductance matrix, $[K]$ (or $[L]^{-1}$), is not proportional to capacitance matrix, $[C_0]$, $[K]$ may still have similar local property as $[C_0]$. If this is true, then we can apply K extraction locally, and derive RKC equivalent circuit models, instead of RLC models to model the inductance effect.

Here, we should emphasize that $[L_{loop}]$ have complete different meaning with $[L]$. The element in $[L_{loop}]$ is loop inductance, and it was calculated with a pre-defined ground return path. That is to say, there is only an $(n-1) \times (n-1)$ $[L_{loop}]$ matrix for an n conductor system. While the element in L matrix is partial inductance, and it was assumed all current return in infinity. For an n conductor system, an $n \times n$ L matrix is obtained. Therefore, although, the K matrix has similar locality as the C matrix, it is not related to the capacitance matrix.

3.2 Locality of K

The following example demonstrate the locality of K matrix. Consider a layout example with five parallel buses, shown in Fig. 2. The length of all buses is 20 μm, the cross section is 2x2 μm, and the spacing between the buses is 5 μm.
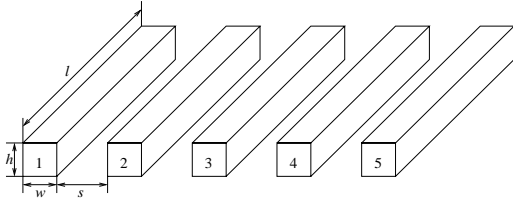

Figure 2: Layout Example with 5 Parallel Buses

We calculated the partial inductance matrix, L, using FastHenry [5],

$$[L] = \begin{bmatrix} 11.4 & 4.26 & 2.54 & 1.79 & 1.38 \\ 4.26 & 11.4 & 4.26 & 2.54 & 1.79 \\ 2.54 & 4.26 & 11.4 & 4.26 & 2.54 \\ 1.79 & 2.54 & 4.26 & 11.4 & 4.26 \\ 1.38 & 1.79 & 2.54 & 4.26 & 11.4 \end{bmatrix} \quad pH, \quad (7)$$

and then inverted L to get K matrix.

$$[K] = \begin{bmatrix} 103 & -34.1 & -7.80 & -4.31 & -3.76 \\ -34.1 & 114 & -31.6 & -6.67 & -4.31 \\ -7.80 & -31.6 & 115 & -31.6 & -7.80 \\ -4.31 & -6.67 & -31.6 & 114 & -34.1 \\ -3.76 & -4.31 & -7.80 & -34.1 & 103 \end{bmatrix} \times 10^9 H^{-1}$$

$$(8)$$

From Eq. (7) and Eq. (8), we can see that the partial mutual inductance L_{51} is 1.38/11.4 or 12.1% of the partial self inductance L_{11}, while $|K_{51}|$ is only 3.76/103 or 3.7% of the self term K_{11}.

Meanwhile, we also calculated the capacitance matrix

of the above structure shown in Fig. 2 using FastCap [10].

$$[C] = \begin{bmatrix} 555 & -202 & -43.8 & -23.5 & -20.9 \\ -202 & 631 & -187 & -37.0 & -23.5 \\ -43.8 & -187 & 634 & -187 & -43.9 \\ -23.5 & -37.0 & -187 & 631 & -202 \\ -20.9 & -23.5 & -43.9 & -202 & 555 \end{bmatrix} \quad pF$$

$$(9)$$

It can be observed the amazing similarity of the decreasing trend of the off-diagonal elements in both K and C matrix. For example, the absolute value of mutual capacitance $|C_{51}|$ is about 20.9/555 or 3.8% of the self capacitance C_{11}.

That is to say, the off-diagonal elements in K matrix decrease faster than that of the partial inductance matrix, and at a similar speed as that in capacitance matrix, which we call K matrix has locality. The physical explanation of this locality for K matrix is provided in [1].

3.3 K-based method

Since K has locality, we only need to consider a small number of conductors enclosed in small window when extracting K. Our approach can be summarized as follows.

- Calculate the partial inductance matrix, L, of a small structure which is enclosed in a small window.
- Calculate the small K matrix by inverting the corresponding L matrix.
- Compose the big K_{all} matrix by the column in each small K matrix, which is corresponding to the aggressor, like the techniques used in capacitance extraction.
- Simulate the subsequent RKC equivalent circuit.

As we mentioned before, in order to be a practical approach, K-based method has to guarantee the stability of the subsequent RKC equivalent circuit. The proof of the stability abide by the following steps [1]:

- K matrix in general is diagonal dominant.
- The sparse K_{all} matrix constructed by K-based method is still diagonal dominant.
- K_{all} matrix is positive definite. Therefore, the subsequent RKC equivalent circuit is stable.

Due to space limitation, please reference [1] for detailed proof.

Therefore, for a large system, K-based method will generate a very sparse and stable system in later circuit simulation. Thus it can save a great amount of CPU time and memory usage when capturing on-chip inductance effect.

4 Experiment Results

To simply illustrate the accuracy of K-based method, we still use the 5 parallel buses example shown in Fig. 2. We calculate the loop inductance between bus 1 and 5 with and without the coupling term K_{15}. That is we calculate the loop inductance between bus 1 and 5 associated with matrix $[K]$ and $[K']$, stated in Eq. 8 and Eq. 10, respectively. Since directly calculating loop inductance using K

matrix involves complicated calculation, we use the corresponding partial inductance matrices, $[L]$ and $[L']$, stated in Eq. 7 and Eq. 11, respectively.

$$[K'] = \begin{bmatrix} 103 & -34.1 & -7.80 & -4.31 & 0 \\ -34.1 & 114 & -31.6 & -6.67 & -4.31 \\ -7.80 & -31.6 & 115 & -31.6 & -7.80 \\ -4.31 & -6.67 & -31.6 & 114 & -34.1 \\ 0 & -4.31 & -7.80 & -34.1 & 103 \end{bmatrix} \times 10^9 H^{-1}$$
(10)

$$[L'] = \begin{bmatrix} 11.3 & 4.17 & 2.42 & 1.60 & 0.89 \\ 4.17 & 11.4 & 4.20 & 2.46 & 1.60 \\ 2.42 & 4.20 & 11.4 & 4.20 & 2.42 \\ 1.60 & 2.46 & 4.20 & 11.4 & 4.17 \\ 0.89 & 1.60 & 2.42 & 4.17 & 11.3 \end{bmatrix} pH,$$
(11)

As we all know, $L_{loop15} = L_{11} + L_{55} - L_{15} - L_{51}$. With the coupling term K_{15}, we get $L_{loop15} = 2 \times (11.4 - 1.38) = 20.04pH$. Without the coupling term K_{15}, we get $L'_{loop15} = 2 \times (11.3 - 0.89) = 20.82pH$, which is 3.9% more than the exact value L_{loop15}. However, if we approximate L_{loop15} by directly ignoring L_{15} in $[L]$ matrix, we will get $L''_{loop15} = 2 \times 11.4 = 22.8pH$, which is 13.8% overestimation, a much larger error compared to K-base method.

Next, consider the two power planes depicted in Fig. 3. This is the same example presented in Fig. 5 of [7]. When power plane inductance and K matrix are modeled, power planes such as these are meshed into separate x and y conductor segments. (Even solid power planes are meshed into separate x and y conductors.) Because orthogonal conductors do not couple magnetically, the resulting inductance matrix and K matrix are block diagonal matrices.
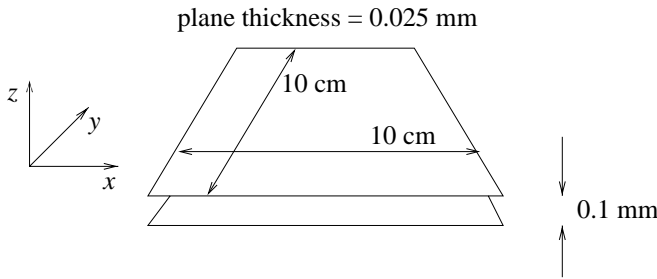
plane thickness = 0.025 mm

Figure 3: Two Power Planes for Inductance Effect Modeling

To compare our approach with the conventional and the shift-truncate method in [7], we calculate the eigenvalues of partial inductance matrix in the conventional and the shift-truncate method by strictly following Krauter's paper [7].

That is, for the two planes depicted in Fig. 3, we created, using FastHenry [5], a partial inductance matrix to model the magnetic coupling in the x direction. Each plane was

meshed into 100 equal 10 mm square segments along the x direction, and uniform current flow was assumed along all segments (FastHenry parameters nhinc and nwinc were set to one).

Firstly, to visualize the decrease speed of the off-diagonal elements in L matrix and K matrix, we plotted the normalized mutual couplings between the left-bottom most segment and other segments in the same power plane with respect to the self term of the left-bottom most segment for both L and K matrix, depicted in Fig. 4 and Fig. 5, respectively. We observed that the off-diagonal elements in K matrix decrease much faster than those of the partial inductance matrix, which again illustrated the locality of K matrix compared to L matrix. Since K has locality, we only need to consider a small number of conductors enclosed in small window when extracting K.
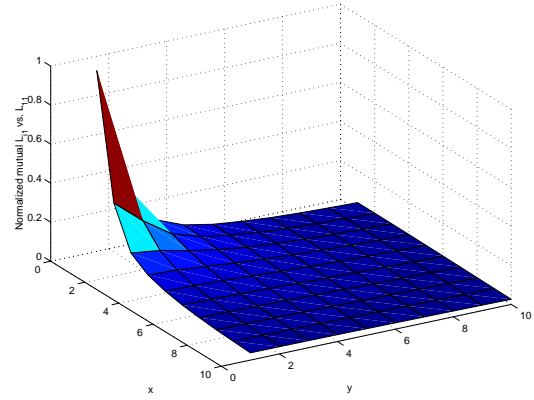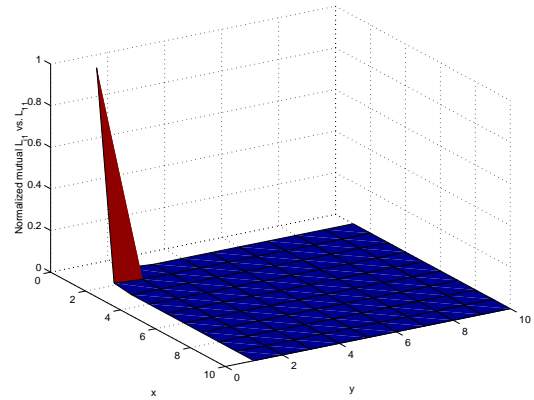

Figure 4: Normalized mutual couplings between the left-bottom most segment and other segments in the same power plane with respect to the self term of the left-bottom most segment for L matrix

Figure 5: Normalized mutual couplings between the left-bottom most segment and other segments in the same power plane with respect to the self term of the left-bottom most segment for K matrix

Secondly, from this FastHenry partial inductance matrix, we created two sparse approximations of the full matrix. The first approximation was formed using the shift-truncate procedure. That is, we set the current return radius r_0 equal to 12 mm, and when the result was negative, the matrix term was set to zero. The projection on x-y coordinate of the small representing structure enclosed in the current return shell is shown in Fig. 6.
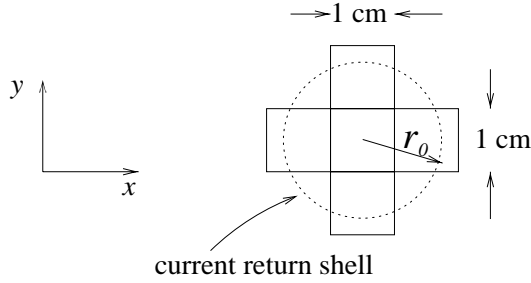

Figure 6: The Representing Structure in Modeling the Two Power Planes

The second sparse approximation was formed by discarding all mutual inductances less than 0.75 nH. In both cases, 38,160 of the total 40,000 matrix terms were set to zero, (*i.e.* both approximations were > 95% sparse). Finally, the eigenvalues of the full matrix and the two sparse approximations were computed. The 200 eigenvalues for each matrix are plotted in Fig. 7.
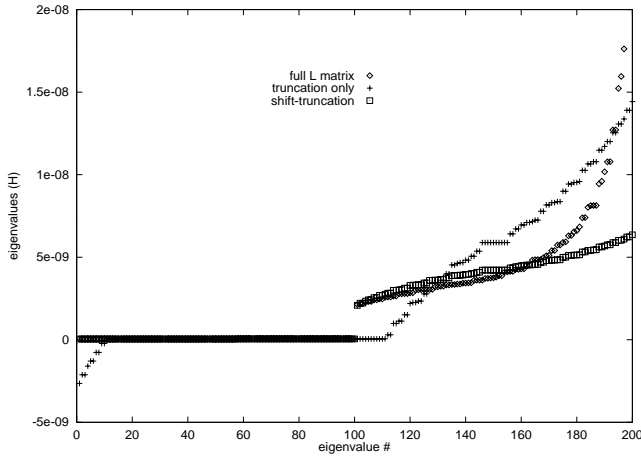

Figure 7: Eigenvalues for Full and 95% Sparse L Matrices Modeling the Two Power Planes in Fig. 3

In our K-based approach, we calculated the K matrix of the conductor segments included in the small window as those enclosed in the current return shell in shift-truncate method to ensure same sparsity. Therefore, the whole K system has exactly same sparsity (> 95%) as those in shift-truncate and truncation only method. Since K matrix is the inverse of L matrix, the eigenvalues of K matrix should

also be the inverse of those of L matrix. For better illustration, we plotted the inverse of K's eigenvalues in Fig. 8.

In observing Fig. 7, note that the approach of simply discarding the smallest terms in the inductance matrix, yields both an inaccurate and an unstable approximation as it fails to match the eigenvalues of the full matrix at both extremes and in the middle. Although the smallest 100 eigenvalues of the shift-truncate method match those of the full L matrix, and shows the same discontinuous jump between the 100th and 101st eigenvalue, there are significant difference for larger eigenvalues between the shift-truncate method and the full matrix.
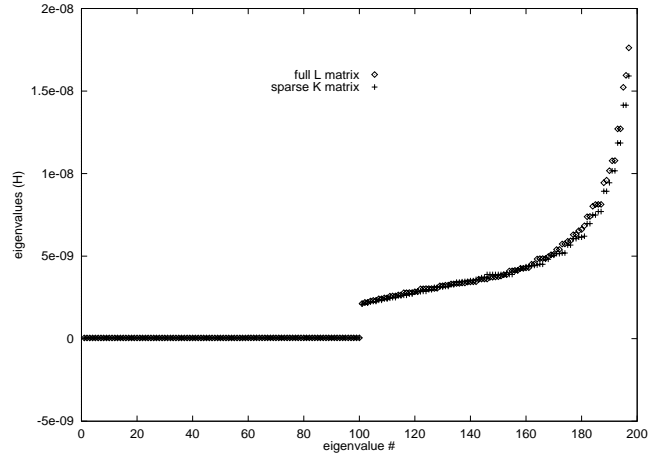

Figure 8: Eigenvalues for Full L matrix and 95% Sparse K Matrix Modeling the Two Power Planes in Fig. 3

Fig. 8 shows the excellent match of the eigenvalues between sparse K matrix and full L matrix.

Finally, to compare the effects of full inductance matrix and sparse K matrix in circuit simulations, we choose a structure presented in Fig. 8(b) of Krauter's paper [7]. The circuit is illustrated in Fig. 9. We deliberately chose this circuit topology because the current loops were larger than that in Fig. 8(a) of Krauter's paper [7]. Thus, it will be more obvious whether or not the K-based method can capture enough mutual inductance coupling. In this structure, each conductor has cross section of 2x2 μm square, $d_1 = 10\mu$m, $d_2 = 40\mu$m, and $d_3 = 1600\mu$m. Each conductor was broken into forty equal segments in order to create a large yet illustrative partial inductance matrix.

To make the inductive effects dominate, R_s and R_t were set to 1 and 10 ohms, and a rise time (0.1ns) was employed to simulate the frequency of on-chip interconnect application.

In our approach, the window size was assumed to include at most 3 segments of each conductor. The sparsity of the resulted K matrix is about 92.6%. The circuit simulation is performed by Ksim [1], which simulates RKC equivalent circuit, instead of RLC. The simulation results is shown in Fig. 10. We can see good agreement in terms
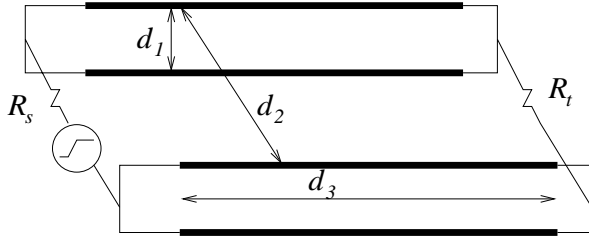
Figure 9: Circuit Example same as Fig. 8 from Krauter's paper[7]

of circuit simulation results between the full L matrix and the sparse K matrix.
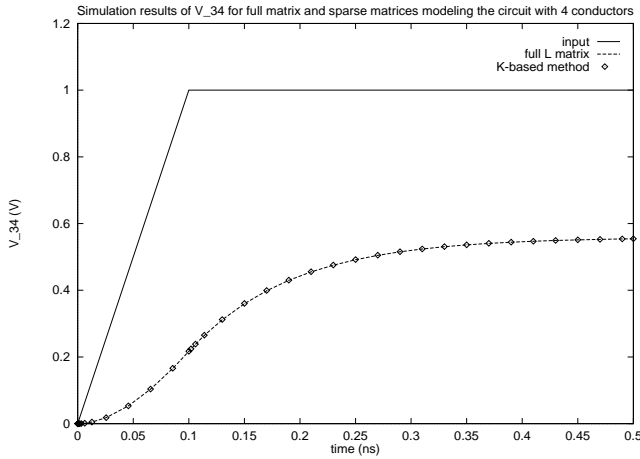

Figure 10: Simulation Results for Circuit Example in Fig. 9

5 Conclusion

Partial inductance are extremely useful in modeling circuit inductances when the induced current loops are unknown. Unfortunately, these matrices are dense and defy conventional simplifications (i.e. the smallest matrix cannot be indiscriminately discarded).

In this paper, we introduce a new circuit element, K, as the inverse of partial inductance. We found out that K is capable of capturing inductance effect, while still preserve locality. Since K matrix is a sparse diagonally dominant matrix, we only need to consider a small number of neighbors. Therefore, we proposed to capture on-chip inductance effect by directly extracting and simulating K, instead of partial inductance. As the result, the K matrix for circuit simulation is very sparse. Thus it can save a great amount of CPU time and memory usage when capturing on-chip inductance effect. This new concept has been verified by the simulation results of practical examples, and showed remarkable accuracy over other sparsification techniques, such as the shift-truncate method and

truncation only method.

We further understand the physical meaning of K and the reason that K has local property [1]. Most importantly, it can be proved that the sparse system matrix constructed by ignoring far away mutual K is positive definite [1].

Therefore, we can later construct libraries or analytical formulas for K, which will enable this K-based method to be a practical one to predict and capture inductance effect for the whole chip.

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