Power Estimation For A Submicron CMOS Inverter Driving A CRC Interconnect Load

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ABSTRACT

We present an analytical expression for the evaluation of the short-circuit power dissipation in a CMOS inverter driving a CRC interconnect load. The validity of the model is much improved over previous works that inaccurately model a MOS transistor as a piecewise linear element, inadequately consider short-circuit current, or inappropriately apply the total capacitance approach. Moreover, our method requires less characterization effort while considering short-channel effects and secondary effects such as short-circuit current and coupling capacitance. As a result of this analysis, the results from proposed model are very close to those of SPICE3.

Categories and Subject Descriptors

J.6 [**Computer Applications**]: Computer-Aided Engineering; B.7.2 [**Integrated Circuits**]: Design Aids—*power estimation*

General Terms

Design, Verification

1. INTRODUCTION

The growing demand for low-power portable computing systems has made power consumption a critical parameter in VLSI chip designs. Moreover, as chips are becoming larger and denser, interconnects play a dominant role in the overall VLSI chip performance. Therefore, the main goal of this work is the derivation of an analytical expression for the short-circuit power dissipation of a CMOS inverter driving a interconnect load.

Most of the timing and power modeling techniques for gates driving RC interconnects can be commonly divided into two broad classes. The first class of methods simplifies the gate modeling by treating the nonlinear MOS transistors as linear or piecewise linear elements such as a Thevenin equivalent voltage source in series with a single resistor [4], [5]. Because of fundamental inaccuracy in modeling a MOS transistor as a piecewise linear element, especially for submicron devices, this is a major shortcoming of this method. Moreover, the computational advantage over a circuit simulator is not very significant.

The second class of methods preserves the driver circuit, but models the RC effects of the interconnect using the effective load. Much research effort has been devoted to the analytical estimation in CMOS gates driving simple total capacitance that represents the RC interconnect [14], [16], [2], [3], [8], [9]. Since a large portion of the power dissipation and signal delay is due to the effects of the RC interconnect, this approximation results in limited accuracy. To overcome this disadvantage, two approaches have been developed. In one approach [1], [7], the interconnect is reduced to an equivalent L-model: a load modeled simply by a resistor in series with a capacitor. In addition to the driving transistor considered to operate always in linear region, step input and negligible short circuit current was examined, thus leading to significant errors [1]. In a different approach [13], [10], [12], the RC interconnect is reduced to an equivalent CRC π-model load. In [13], an effective capacitance was calculated by an iteration procedure and some portion of the output response is achieved by a simple but inaccurate resistive model. Hirata [10] derived the output ramp response, where the short-circuit current was approximated with a piecewise linear function to estimate the short-circuit power dissipation then timing delay model, and the delay is calculated in a numerical way for some cases. In [12], the analytical expression for the CMOS inverter driving equivalent CRC π-model with the assumption of the symmetrical PMOS current is valid only for fast input ramps. For the case of very lightly loading and/or slow input ramp, the results lead to inaccuracies.

In this work, an analytical expression for the evaluation of the short-circuit power dissipation in a CMOS inverter, based on the Shoji's MOS model [15] that includes short-channel effects such as the carriers velocity saturation effect, is derived in order to overcome the weaknesses of previous works. A reduced-order π-model is used in this work, since it provides better accuracy than the L-model [1], [7], [6] and the total capacitance approach [2], [9]. Moreover, our method requires less characterization effort and less computational time while considering short-channel effects and
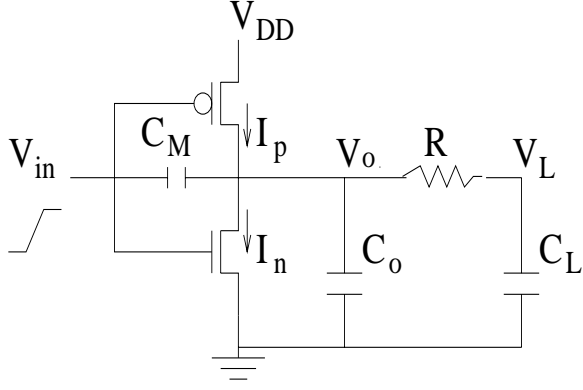
Figure 1: The CMOS inverter driving CRC interconnect loads.

Figure 2: Operation regions in four cases of input ramps.

secondary effects such as short-circuit current and coupling capacitance.

2. THE STATE EQUATION AND SHOJI'S SHORT-CHANNEL CURRENT MODEL

In Fig. 1, the output voltage response for the CMOS inverter driving CRC π load can be expressed by

$$V_o = V_L + RC_L \frac{dV_L}{dt} \qquad (1)$$

$$C_2 \frac{d^2 V_L}{dt^2} + \frac{dV_L}{dt} - H(t-t_r)C_3 \frac{dV_{in}}{dt} + \frac{I_n - I_p}{C_1} = 0 \qquad (2)$$

where $H(t - t_r) = 1$ if $0 < t \leq t_r$, $H(t - t_r) = 0$ if $t > t_r$, $C_1 = C_L + C_o + C_M$, $C_2 = \frac{RC_L(C_o + C_M)}{C_1}$, and $C_3 = \frac{C_M}{C_1}$. The propagation delays are then computed as the time to charge the load capacitance through the P-channel transistor (for the output rising response) and the time to discharge the load capacitance through the N-channel transistor (for the output falling response). The derivation we developed here will be solved only for the output falling response with input rise time t_r, but similar expressions can easily be obtained for the output rising response.

The Shoji's model [15] has been used for the transistor currents to take into account various short-channel effects such as velocity saturation that were ignored in previous works.

$$I_{DS} = \begin{cases} 0 & V_{GT} \leq 0 \\ \beta V_C V_{GT} & V_{DS} \geq V_{DSAT} \\ \frac{\beta}{1 + V_{DS}/V_C}(V_{GT} - \frac{V_{DS}}{2})V_{DS} & V_{DS} \leq V_{DSAT} \end{cases} \qquad (3)$$

where $V_{GT} = V_{GS} - V_{th}$, and $V_{DSAT} = V_C(\sqrt{1 + \frac{2V_{GT}}{V_C}} - 1)$. The normalized saturation voltage for NMOS and PMOS are given by

$$u_{don}(x) = v_{cn}(\sqrt{1 + \frac{2(x-n)}{v_{cn}}} - 1)$$

and

$$u_{dop}(x) = v_{cp}(\sqrt{1 + \frac{2(1-x-p)}{v_{cp}}} - 1).$$

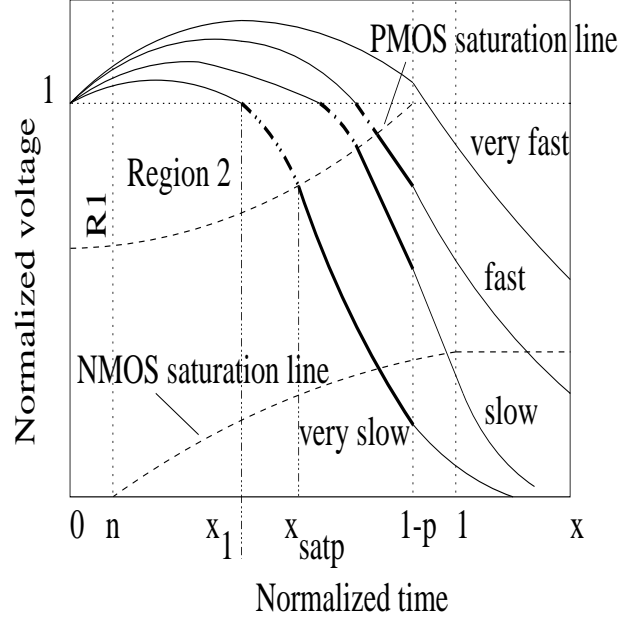To give a complete analysis, four cases of input ramps (i.e., very fast, fast, slow, and very slow) are considered. For plotting purpose, normalized voltages with respect to V_{DD}, i.e., $v_o = V_o/V_{DD}$, $v_L = V_L/V_{DD}$, $n = V_{tn}/V_{DD}$, $p = V_{tp}/V_{DD}$, $u_{don} = V_{DSATn}/V_{DD}$, $u_{dop} = V_{DSATp}/V_{DD}$, and the normalized time $x = t/t_r$ are used, as shown in Fig. 2.

3. TRANSIENT ANALYSIS

The above differential equations are solved resulting in the expressions for the output voltage waveform for each operating region of the transistors.

Region 1.(R1) $0 \leq x \leq n$: The PMOS is linear and the NMOS is off in this region. Because of the small value of drain-source voltage of the PMOS device, the quadratic term and V_{DS} at the denominator of the PMOS current are ignored. In the meantime, the average current of PMOS transistor (i.e., setting $x_1 = n/2$) is used to obtain analytical solution. If $z > 0$, the solution is

$$v_{L,1}(x) = \frac{1}{V_{DD}}(c_{11} e^{y_1 t} + c_{12} e^{y_2 t} + V_p) \qquad (4)$$

where $V_p = \frac{C_4 + k_1 V_{DD}}{k_1}$, $k_1 = \frac{B_p V_{DD}(1 - x_1 - p)}{C_1(1 + v_{ds}/v_{cp})}$, $p_1 = 1 + k_1 RC_L$, $p_2 = 4k_1 C_2$, $z = p_1^2 - p_2$, $y_1 = \frac{-p_1 + \sqrt{z}}{2C_2}$, $y_2 = \frac{-p_1 - \sqrt{z}}{2C_2}$, $c_{12} = \frac{y_1 V_{DD} - V_p}{y_1 - y_2}$, and $c_{11} = \frac{-y_2 c_{12}}{y_1}$. If $z < 0$, the solution is

$$v_{L,1}(x) = \frac{1}{V_{DD}}[e^{pt}(c_{13} cos(qt) + c_{14} sin(qt)) + V_p] \qquad (5)$$

where $c_{13} = V_{DD} - V_p$, $c_{14} = \frac{-pc_{13}}{q}$, $p = \frac{-p_1}{2C_2}$, and $q = \frac{\sqrt{-z}}{2C_2}$.

Region 2.(R2) $n \leq x \leq 1 - p$ for very fast input ramp, otherwise $n \leq x \leq x_{satp}$: The PMOS is still in linear region while the NMOS enters saturated region. Since node differential equation (2) can not be solved analytically, linear approximation is used to obtain more accurate solution. Fig. 3 illustrates this approach. The analytical solution with
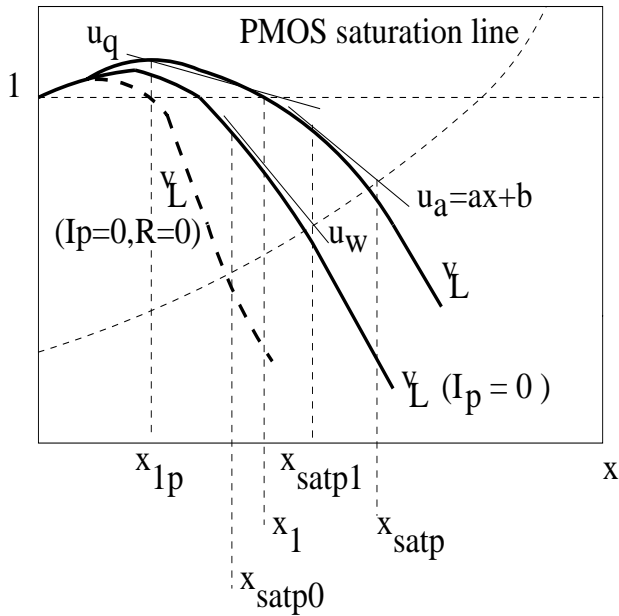
Figure 3: Evaluation of the normalized time x_{satp} and x_1.

the assumption of negligible PMOS current and resistance R can be easily obtained by

$$v_{L,2z}(x) = v_{L,1}(n) + c_m(x-n) - \frac{A_{n1}v_{cn}(x-n)^2}{2} \quad (6)$$

where $A_{n1} = \frac{V_{DD}t_r}{C_L + C_o + C_M}$. With the assumption of negligible PMOS current and resistance R, the normalized time value x_{satp0} can be obtained by Taylor series expansion around x=(1-p+n)/2 up to the second-order coefficient due to the saturation condition $v_{L,2z} = 1 - u_{dop}$ (Fig. 3).
If only negligible PMOS current is assumed in this region, the analytical solution of the differential equation is

$$V_p = C_4 t - \frac{k_3 V_{DD} t_r (x-n)^2}{2}$$
$$- C_2[C_4 - k_3 V_{DD}(x-n)] - \frac{C_2^2 V_{DD} k_3}{t_r} \quad (7)$$

$$v_{L,2p}(x) = \frac{1}{V_{DD}}(k_1 + k_2 e^{\frac{(t_0-t)}{C_2}} + V_p) \quad (8)$$

where

$$k_3 = \frac{\beta_n V_{DD} v_{cn}}{C_1},$$

$$k_2 = -C_2[V'_{L,1}(t_0) - V'_p(t_0)],$$

and

$$k_1 = V_{L,1}(t_0) - V_p(t_0) - k_2.$$

Note that t_0 is initial time, i.e., $t_0 = nt_r$. The tangent of approximated output waveform $v_{L,2p}$ is calculated by

$$u_{2w} = v_{L,2w}(x) = wx + y$$

where $w = v'_{L,2p}(x_{satp0})$ and $y = v_{L,2p}(x_{satp0}) - wx_{satp0}$. The normalized time value x_{satp1} with the assumption of

negligible PMOS current is computed by using Taylor series expansion around x=(1-p+n)/2 up to the second-order coefficient since they satisfy condition $u_{2w} = 1 - u_{dop}$.
Assuming the PMOS current is linear between $x = x_c$ and $x = n$, the PMOS current is approximated by $I_{p1} = I_{pmin} + S(x-n)$ with the slope S and initial current I_{pmin}. For most of cases, $x_c = \frac{1-p+n}{2}$. However, this leads to inaccuracy in the case of extremely slow input ramp. To solve this problem, $x_c = x_{satp0}$ or $x_c = x_{satp1}$ is used to obtain more accurate PMOS current. As shown in Fig. 4, these values are computed by the following expressions:

$$v_{dn} = v_{L,1}(n) + RC_L v'_{L,1}(n)$$

$$v_{dc} = v_{L,2p}(x_c) + RC_L v'_{L,2p}(x_c)$$

$$I_{pmin} = I_p(n, v_{dn})$$

$$I_c = I_p(x_c, v_{dc})$$

$$S = \frac{I_c - I_{pmin}}{x_c - n}$$

After solving differential equation (2) with the approximated PMOS current I_{p1}, output waveform is described by

$$V_p = C_{4b} t - \frac{k_{3b} V_{DD} t_r (x-n)^2}{2}$$
$$- C_2[C_{4b} - k_{3b} V_{DD}(x-n)] - \frac{C_2^2 V_{DD} k_{3b}}{t_r} \quad (9)$$

$$v_{L,2}(x) = \frac{1}{V_{DD}}(k_1 + k_2 e^{\frac{(t_0-t)}{C_2}} + V_p) \quad (10)$$

where

$$k_{3b} = \frac{\beta_n V_{DD} v_{cn}}{C_1} - \frac{S}{V_{DD} C_1},$$

$$C_{4b} = C_4 + \frac{I_{pmin}}{C_1},$$

$$k_2 = -C_2[V'_{L,1}(t_0) - V'_p(t_0)],$$

and

$$k_1 = V_{L,1}(t_0) - V_p(t_0) - k_2.$$

The value x_{satp} is normalized time when PMOS transistor is entering the saturation region. In order to obtain more accurate x_{satp}, the tangent of exact output waveform is calculated by $u_{2a} = ax + b$, where $a = v'_{L,2}(x_{satp1})$ and $b = v_{L,2}(x_{satp1}) - ax_{satp1}$ (Fig. 3). The second order Taylor series expansion around x=1-p-n can then be used to solve x_{satp} since it satisfy saturation condition $u_{2a} = 1 - u_{dop}$.

4. SHORT-CIRCUIT POWER DISSIPATION

The short-circuit power dissipation is given by

$$P_{sc} = f(E_F + E_R),$$

where f is the switching frequency. E_F and E_R are the energy dissipation per falling and rising output transition, respectively. For a falling output transition, short-circuit power is dissipated from the end of the output voltage overshoot $(x = x_1)$ until the PMOS device is turned off $(x = 1 - p)$
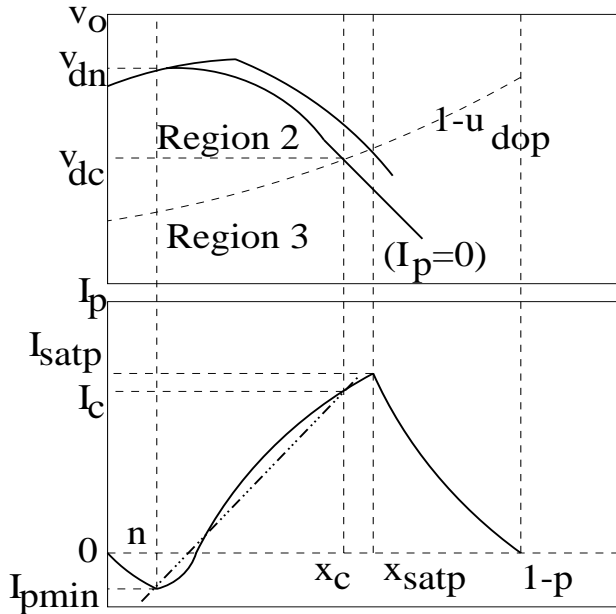
Figure 4: The approximated PMOS current in Region 2.

[2], as shown in Fig. 2. In the case of very fast input ramp, there is no short-circuit power dissipation since the PMOS devices have been turned off before the end of the overshoot. In other cases of input ramps, E_F is then expressed as

$$E_F = V_{DD} t_r \left(\int_{x_1}^{x_{satp}} I_p dx + \int_{x_{satp}}^{1-p} I_p dx \right).$$

The approximated current I_{p1} discussed in region 2 can be used for the period between x_1 and x_{satp} while the PMOS saturation current is used in the second integral. By substituting I_p into it, the short-circuit energy dissipation is

$$
\begin{aligned}
E_F(x) &= V_{DD} t_r [I_{pmin} x + \frac{S}{2}(x-n)^2] \Big|_{x_1}^{x_{satp}} \\
&+ \frac{V_{DD}^3 t_r \beta_p v_{cp}}{2}(1-p-x_{satp})^2 \quad (11)
\end{aligned}
$$

During the output voltage overshoot (i.e., V_o is higher than V_{DD}), there is no current from power supply to ground so that no short-circuit power is dissipated. The value x_1 is normalized time when the end of the overshoot occurs. In order to obtain more accurate x_1, similar approach discussed in Region 2 is applied (Fig. 3). The normalized time value x_{1p} with the assumption of negligible PMOS current and resistance R is computed by using Taylor series expansion around $x = (1-p+n)/2$ up to the second-order coefficient since it satisfy condition $v_{L,2z} = 1$. Assuming the output waveform is linear between $x = x_{1p}$ and $x = x_1$, the output voltage is approximated by

$$u_{2q} = v_{L,2q}(x) = px + q$$

where $p = v'_{L,2}(x_{1p})$ and $q = v_{L,2}(x_{1p}) - px_{1p}$. Therefore, $x_1 = (1-q)/p$ since it satisfy condition $u_{2q}(x_1) = 1$. Similarly, E_R can be easily obtained by exchanging NMOS parameters with PMOS ones, where x_1 is normalized time value when the end of the output voltage undershoot occurs.

Table 1: Typical MOS model parameters.

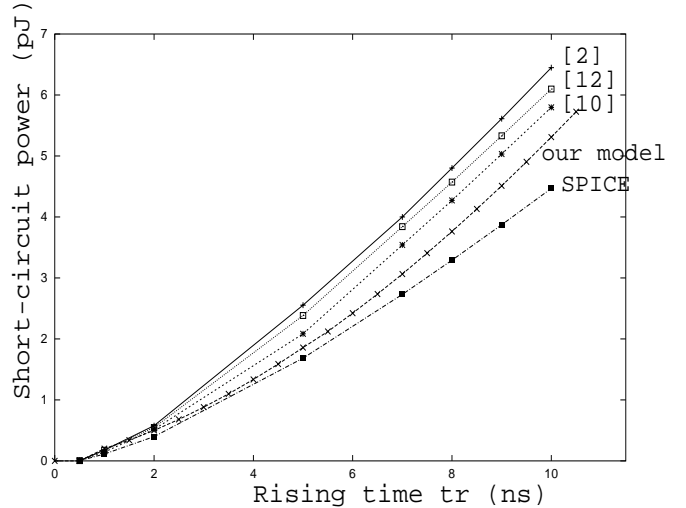| SPICE Model	BSIM3(0.35um)	
Proposed Model	MS(0.35um)	
parameters	NMOS	PMOS
$width$	1um	2um
I_{DO}	1.300E-03	-1.531E-03
V_{th}	0.579412	-0.6070171
μ_0	400.4844971	134.8771109
t_{ox}	7.6E-9	7.6E-9
V_c	0.62	0.85

Figure 5: Short-circuit power dissipation of the CMOS inverter driving a CRC π load using the proposed model and SPICE (BSIM3).

5. SIMULATION RESULTS

In this section, we compare the results for a CMOS inverter driving CRC interconnect loads for various conditions of output loading and input signal rise time t_r. In addition to typical SPICE dc model parameters, parasitic capacitances are added to the model descriptions, as shown in Table 1. Part of simulation results are shown in Fig. 5, where the inverter loaded by $C_o = 0.1pF$, $R = 0.1k\Omega$, and $C_L = 0.6pF$. In order to demonstrate the accuracy advantage of the proposed short circuit power dissipation model, Fig. 5 shows the presented approach gives results closer to those obtained from SPICE simulations than previous works [10], [12], [2]. The SPICE results have been obtained by using the powermeter subcircuit [11], [17]. This is achieved because the proposed technique use more accurate PMOS current than those used in previous works [10], [12], where either fully linearized PMOS current is used [10] or symmetrical PMOS current is assumed [12]. Moreover, the short circuit power dissipation model with CRC loading is more accurate than that with total capacitance [2] and than that with RC L-model [1], where 40% error has been reported.

6. CONCLUSION

We present the analytical expressions for the short-circuit power dissipation of a CMOS inverter driving CRC interconnect loads. The validity of the model is much improved over previous works that neglect the influence of the coupling capacitance, the short-circuit current, and velocity saturation.

The analysis is based on a relatively simple short-channel current model, but it gives good physical insight into the power dissipation problem of a CMOS inverter driving a CRC π load. The accuracy advantage has been demonstrated under many loading conditions and input rise times without recharacterization. Instead of using total capacitance model, the shortcoming of such high accuracy and wide applicability is an increased computation time due to more complicated closed-form solutions.

7. REFERENCES

[1] V. Adler and E. Friedman. Delay and power expressions for a CMOS inverter driving a resistive-capacitive load. In *Proc. IEEE Int. Symp. Circuits and Systems*, pages 101–104, May 1996.

[2] L. Bisdounis, S. Nikolaidis, and O. Koufopavlou. CMOS short-circuit power dissipation including velocity saturation and gate-to-drain capacitive coupling. In *Sixth Int. Workshop on Power and Timing Modeling, Optimization and Simulation*, pages 157–166, Sept. 1996.

[3] L. Bisdounis, S. Nikolaidis, and O. Koufopavlou. Analytical transient response and propagation delay evaluation of the CMOS inverter for short-channel devices. *IEEE J. Solid-State Circuits*, 33(2):302–306, Feb. 1998.

[4] F. Dartu, N. Menezes, and L. T. Pileggi. Performance computation for precharacterized CMOS gates with RC loads. *IEEE Trans. Computer-Aided Design*, 15(5):544–553, May 1996.

[5] F. Dartu, N. Menezes, J. Qian, and L. Pillage. A gate-delay model for high-speed CMOS circuits. In *Proc., ACM/IEEE Design Automation Conf.*, pages 576–580, June 1994.

[6] N. Gopal, D. Neikirk, and L. Pillage. Evaluating RC-interconnect using moment-matching approximations. In *Proc. IEEE Int. Conf. Computer-Aided Design*, pages 74–77, Nov. 1991.

[7] M. Hafed and N. Rumin. CMOS inverter current and delay model incorporating interconnect effects. In *IEEE Int. Symp. on Circuits and Systems*, pages 86–89, May 1998.

[8] N. Hedenstierna and K. Jeppson. Comments on 'a module generator for optimized CMOS buffers'. *IEEE Trans. Computer-Aided Design*, 12:180–181, January 1993.

[9] A. Hirata, H. Onodera, and K. Tamaru. Estimation of propagation delay considering short-circuit current for static CMOS gates. *IEEE Trans. on Circuits and Systems*, 45(11), Nov. 1998.

[10] A. Hirata, H. Onodera, and K. Tamaru. Proposal of a timing model for CMOS logic gates driving CRC π load. In *Proc. IEEE Int. Conf. Computer-Aided Design*, pages 537–544, Nov. 1998.

[11] S. Kang. Accurate simulation of power dissipation in VLSI circuits. *IEEE J. Solid-State Circuits*, SC-21(8):889–891, Oct. 1986.

[12] S. Nikolaidis, A. Chatzigeorgiou, and E. Kyriakis-Bitzaros. Delay and power estimation for a CMOS inverter driving RC interconnect loads. In *Proc. IEEE Int. Symp. Circuits and Systems*, pages 368–371, May 1998.

[13] J. Qian, S. Pullela, and L. Pillage. Modeling the "effective capacitance" for the RC interconnect of CMOS gates. *IEEE Tran. Computer-Aided Design*, 13(12):1526–1535, Dec. 1994.

[14] T. Sakurai and A. R. Newton. Alpha-power law MOS-FET model and its applications to CMOS inverter delay and other formulas. *IEEE J. Solid-State Circuits*, 25:584–594, April 1990.

[15] M. Shoji. *CMOS Digital Circuit Technology*. Prence-Hall, New Jersey, 1987.

[16] S. R. Vemuru and N. Scheinberg. Short-circuit power dissipation estimation for the CMOS logic gates. *IEEE Trans. Circuits and Systems I*, 41:762–765, Nov. 1994.

[17] G. Yacoub and W. Ku. An enhanced technique for simulating short circuit power dissipation. *IEEE J. Solid-State Circuits*, 24:844–847, June 1989.