SC²L; A Low-Power High-Performance Dynamic Differential Logic Family

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ABSTRACT

A new dynamic differential logic family, Short-Circuit Current Logic (SC^2L), is proposed for low-power high-performance applications. It achieves low-power consumption by using an aggressively reduced logic swing without requiring restoration circuitry. Using a 0.35μm CMOS technology and a nominal supply voltage of 3.3V, a SC^2L full-adder 8 carry ripple adder (CRA) is implemented. It offers an order of magnitude less power-delay product than several other logic families.

Keywords

Digital circuits, high-performance, low-power, low swing logic

1. INTRODUCTION

Perhaps one of the most pervasive trends in advanced digital circuit design is low-power design. Low-power design helps to prolong battery lifetime and reduces heat dissipation in microchips, which aids in reducing packaging costs. Power consumption in any digital design is dominated by dynamic power consumption, which is given as

$$P_{dyn} = \alpha_{0\to1} \cdot C_L \cdot V_{dd} \cdot V_{swing} \cdot f \quad \textbf{(1)}$$

where C_L is the load capacitance, V_{dd} is the supply voltage, V_{swing} is the output logic swing, f is the operating frequency, and $\alpha_{0\to1}$ is the 0→1 data toggling at the output. Reducing the supply voltage trades off speed for lower power consumption. For high-performance applications, such as microprocessors, alternative methods of reducing the power consumption must be explored. In this paper, a new dynamic differential logic family, Short-circuit current logic (SC^2L), provides very high performance at power-delay products an order of magnitude less than other circuit techniques.

2. DYNAMIC DIFFERENTIAL LOGIC FAMILIES

Dynamic logic is usually preferred over static logic in high-performance applications due to its speed advantage. One disadvantage of dynamic differential logic, however, is that it has a switching activity of 1, rendering it incapable of exploiting signal correlation to decrease power consumption. For this reason, dynamic differential logic is usually only used for high-performance systems where signal correlation is low (such as general-purpose computing).

The basic dynamic differential logic structure is also known as dynamic cascode voltage switch (DCVS) logic [5]. It consists of two complementary logic trees, which consists of pull-down NMOS logic trees. The pull-up circuitry consists of two precharge PMOS devices and two cross-coupled PMOS devices. Several variations of this logic family exist such as Differential Current Switch Logic (DCSL) [1] and Sample-Set Differential Logic (SSDL) [2], however, they all contain the same basic configuration with cross-coupled PMOS's or inverters. A Charge Recycling Differential Logic (CRDL) [3] gate is shown in Fig. 1. During the precharge operation, the output and its complement are equalized through MN1, allowing charge to be recycled for the next evaluation cycle. Ideally, 50% of the charge is recycled.

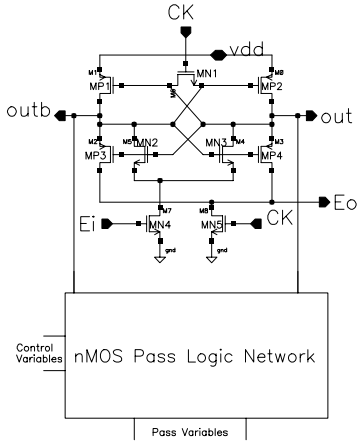

Figure 1. Charge Recycling Differential Logic (CRDL) Gate

3. SHORT-CIRCUIT CURRENT LOGIC

3.1 Basic Operation

The proposed dynamic differential logic family, called Short-Circuit Current (SC^2L) Logic is shown in Fig. 2. Its basic operation is now explained. When CK is high, the CMOS inverter at the bottom (MP1, MN1) discharges node B to 0. This turns on MP2 and MP3. MP4 and MP5 act as pass gates and are turned off for this duration of the clock pulse. The circuit is effectively in precharge mode. During the evaluation mode, the CK input starts to go low. For a brief amount of time, both MP1 and MN1 are turned on. First, the pass gate PMOS transistors are enabled. Secondly, the CMOS inverter dissipates short-

circuit current. This discharges one output through the N-logic tree according to the input logic. The amount of voltage drop across the output is determined by the amount of short-circuit current dissipation, which in turn, depends on the W/L ratio of the pull-down inverter as well as the clock slew rate [4].

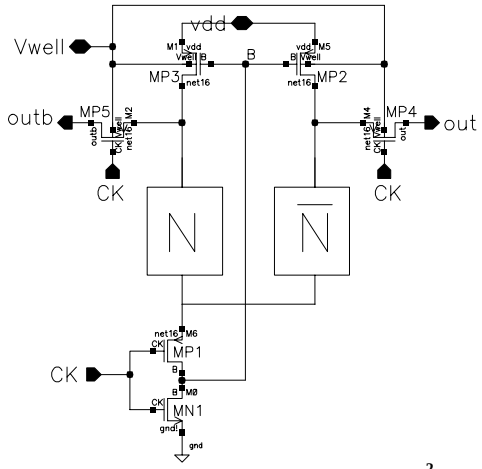

Figure 2. Short-Circuit Current Logic (SC^{2}L) Gate

One important point to note is that the maximum voltage at node B is V_{DD}-$V_{TN,body}$. This means that the body terminals of MP2 and MP3 need to be biased to a boosted supply voltage to effectively them off and the clock swing can be reduced to V_{DD}-$V_{TN,body}$. MP4 and MP5 now must have their body terminals biased to V_{well} since they are driven by a reduced swing clock signal. Reduced clock swing helps in reducing energy consumption and effects of clock feedthrough effect[4], which are serious in reduced swing dynamic logic.

3.2 Modified SC^{2}L Gate

The basic SC^{2}L gate suffers from variation of voltage swing in the presence of variable output loads. One solution entails placing a diode from VDD to the output nodes in order to limit the voltage swing. Although turn on time of the diode is slow, it can be used to hold the output voltages to fixed values at periods of low activity. Fixing the voltage swing also permits the use of charge sharing as in CRDL [3]. This results in a new gate, Quasi-static SC^{2}L (QSC^{2}L), shown in Fig. 3.

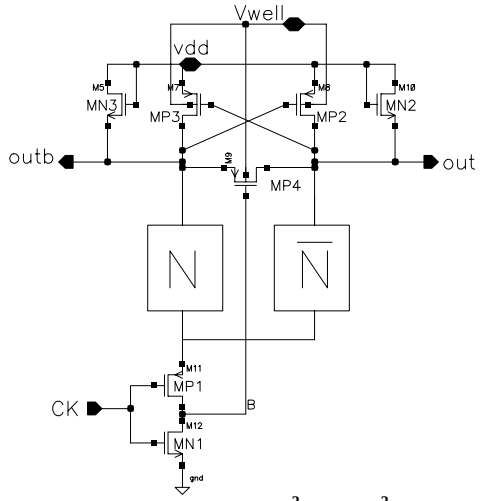

Figure 3. Quasi-static SC^{2}L (QSC^{2}L) Gate

3.3 SC^{2}L Gate Pipelining

One important issue in high-speed dynamic logic design is that of clocking. Distributing the clock signal to every single gate significantly increases the system's clock power. Fig. 4 demonstrates an efficient way to pipeline SC^{2}L gates. In SC^{2}L, the clock is applied only to the first pipeline stage. Subsequent stages receive a completion signal. The completion signal is generated for free. Since node B represents the inversion of the clock signal and it does not fully switch until the output has completely settled, it may be used as a completion signal for the next stage. The disadvantage of this scheme is that it places a larger load on node B, which may slow down circuit operation.

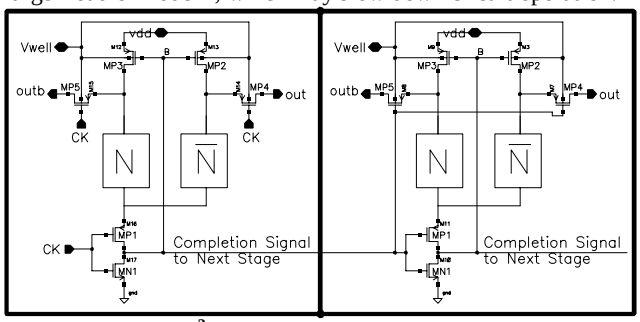

Figure 4. SC^{2}L Asynchronous Pipelining Strategy

4. SC^{2}L SIMULATION RESULTS

In this section, SC^{2}L is evaluated in terms of its delay, power, robustness and is compared to other logic families. All gates were implemented in a 0.35µm CMOS technology.

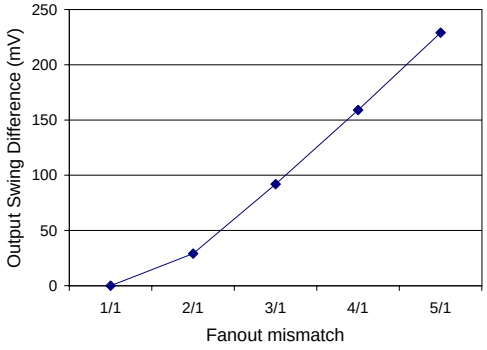

Figure 5. Output voltage swing sensitivity to load mismatch

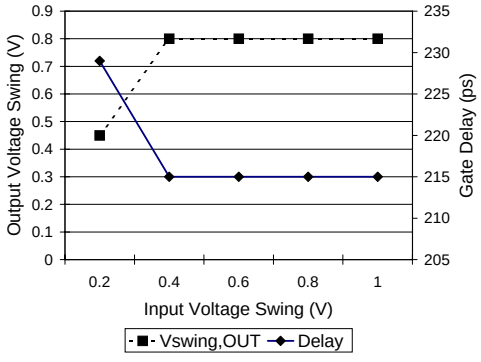

Figure 6. Output voltage swing vs. input voltage swing

Since logic swing is limited by restricting the evaluation time, the output voltage swings may vary according to loading conditions. A SC^{2}L inverter/buffer was used for this characterization with nominal operation conditions of V_{DD}=3.3V, f_{CLK}=500MHz, V_{swing}=0.8V. The output voltage swing sensitivity to fan-out mismatch is shown in Fig. 5. Another important characterization, the output voltage swing and gate's delay sensitivity to input voltage swing, is shown in Fig. 6. As the figure shows, an input voltage swing between 0.4V to 1V causes very little change in the gate's performance. This shows that the gate has good regenerative properties as long as noise injected into the output lines is less than 400mV (0.8V-0.4V).

A full-adder (FA) is used as a benchmark circuit to compare SC^{2}L to other logic styles. Using a fanout of 3 and V_{DD}=3.3V, the results shown in Table 1 have been obtained. As the table reveals, QSC^{2}L has 37% less energy than SC^{2}L, due to charge recycling. SC^{2}L and QSC^{2}L are compared to other logic families (normalized to 100MHz) in Fig. 7. This figure shows that both SC^{2}L and QSC^{2}L exhibit an order of magnitude less power-delay product than other logic families.

Table 1. Results of FA implementation in SC^{2}L and QSC^{2}L

	SC^{2}L (FA)	QSC^{2}L (FA)
Logic Swing	0.7V	0.7V
Frequency	900MHz	900MHz
Power	0.106mW	0.062mW
Energy (uW/MHz)	0.118pJ	0.069pJ
Power-Delay Product	29.15fJ	18.14fJ

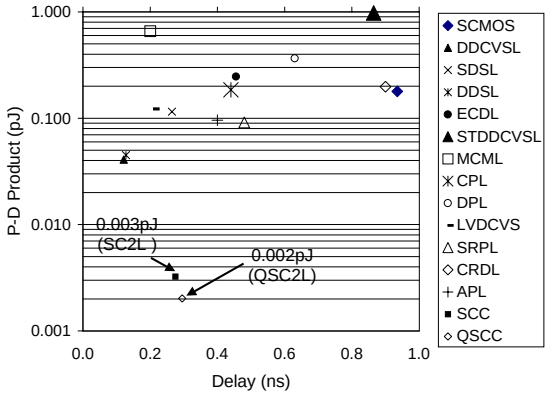

Figure 7. Comparison of SC^{2}L with other logic families

5. SC^{2}L EXPERIMENTAL RESULTS

An 8-bit asynchronous pipelined SC^{2}L-based CRA has been implemented with a target clock rate of 700MHz. Both CRA's were optimized for 0.7V logic swing. In order to ease testing, an on-chip oscillator (CKGEN) and output frequency dividers (DIV2) have been used. Current-mode logic (CML) has been used in the DIV2 circuits to support low-swing inputs. The output's signal (SUM) frequency is divided by 4 to ease testing.

In order to test the functionality of the pipelined CRA, an input vector of A[7:0]=1, B[7:0]=0, and C_{in} alternates between 1 and 0 at one-half the clock frequency, which means that the internal clock rate is running at 8x the output signals' rate. The measured waveform output of the adder is shown in Fig. 8. Since the waveforms display a 90.9MHz operating frequency, the internal clock rate is 727MHz. The measured delay between Sum[7] and Sum[3] is 800ps, which translates to an internal delay of 67ps per FA. The results of the simulated and the measured SC^{2}L FA implementations are compared in Table 2.

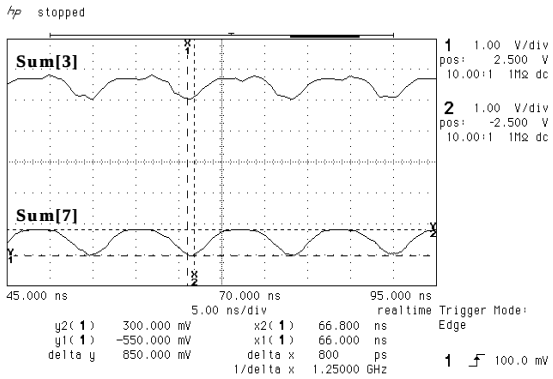

Figure 8. Waveform output of test results from 8bit CRA (Sum[3] and Sum[7] output bits)

Table 2. Simulated & measured results of FA SC^{2}L

SC^{2}L characteristics	Simulated	Measured
Logic Swing	0.7V	0.85V
Frequency	700MHz	727MHz
Delay	80ps	67ps
Power	0.275mW	0.293mW
Energy (uW/MHz)	0.304pJ	0.403pJ
Power-Delay Product	22fJ	19.6fJ

6. CONCLUSIONS

It has been demonstrated that SC^{2}L has great potential for high-speed low-power applications. When using charge recycling with SC^{2}L (QSC^{2}L), 37% energy savings are realized as well as more robust circuit operation, on the expense of extra delay. FA implementations of SC^{2}L and QSC^{2}L have been shown to exhibit an order of magnitude less power-delay product than other logic families. Furthermore, asynchronous pipelining can be used to connect SC^{2}L gates together without introducing any special circuitry. An 8-bit CRA based on this pipelining strategy has been fabricated, tested and found to operate up to 727MHz while dissipating 2.34mW of power.

7. REFERENCES

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