OTA Amplifiers Design on Digital Sea-of-Transistors Array

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Abstract

This paper presents measurement results of OTA (Operational Transconductance Amplifiers) designed in 1.0 m CMOS Digital technology implemented in two different methodologies: in a fixed-size transistors array and in a full-custom design. Some characteristic parameters of OTA's are compared with HSPICE simulations.

1. Introduction

Semi-custom ASIC's using the SOT concept were introduced recently, where the interconnections are placed over the active region leading to flexible designs and effective use of chip area [1], [2], [5]. The SOT offers both short design time and good cost-performance compromise. The challenge then becomes the designing of analog circuits in a conventional gate-isolation digital SOT matrix [3]. Specific techniques for analog design are presented herein, and analog circuits circuits with good performance in SOT are compared to full-custom.

2. OTA Amplifiers

One Miller type OTA and two folded-cascode OTA's were designed in the SOT array. This array was designed for channeless routing for digital circuits, with a single poly level. The OTA type Miller is an amplifier with two stages and is shown in Fig. 1a. Final layout is shown in Fig. 2a. The OTA folded-cascode amplifier schematic is shown in Fig. 1b and the layout is shown in Fig. 4a for full-custom design and in Fig. 4b for the layout in SOT array implementation for the same type of folded-cascode OTA.

Equivalent *W/L* ratio as well as reasonable output resistance could be obtained by having not more than 2 physical transistors in series in the trapezoidal association that emulates a single designed analog transistor [4]. This is supported by the adequate I-V characteristics shown in Fig. 3. A long-channel arbitrary *W/L* full-custom transistor I-V with *L=5 m* is compared to its trapezoidal association counterpart in the same technology, implemented as shown in Fig. 2b.

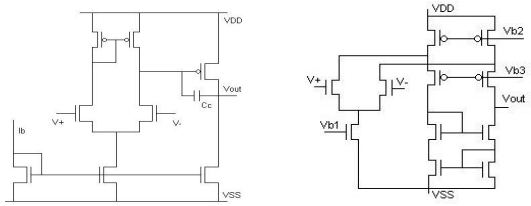

Figure 1: (a) OTA type Miller and (b) Folded-cascode schematic.

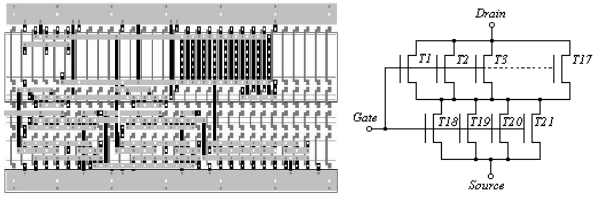

Figure 2: (a) OTA Miller layout. (b) Trapezoidal association of transistor all with *W/L=10.5 m/1.0 m*.

This association improves the output conductance of the FETs with adequate transconductance (g_m) even using minimum channel lengths L_{min}. In Fig. 3, the curve labelled "association" represents the I-V of all transistors connected as shown in Fig. 2b.

3. Tests and Measurements

The results obtained from simulations and measurements in the OTA's designed and fabricated in 1.0µm CMOS are shown in Table 1. It is important to notice that the measured DC voltage gain A_V and gain-bandwidth product (*GBW*) of OTA's are much lower than electrical simulation predictions from Hspice with

level 2 and level 6 models, which attest the weak modelling accuracy for current derivatives (transconductances) provided by digital foundries for minimum-length transistors.

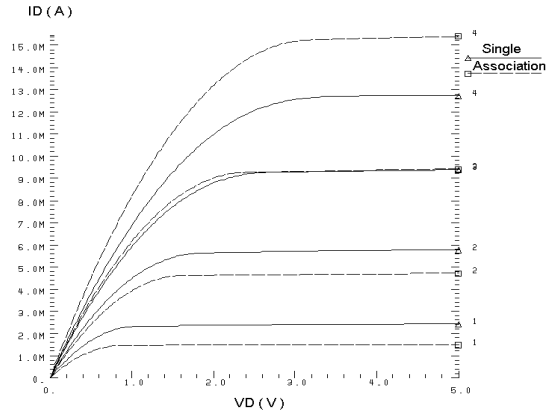

Figure 3: Single and association transistor comparison. Single: *W=170 m, L=5 m, W/L=34*. Association: W_{eq}*=178.5 m,* L_{eq}*=5.25 m,* $(W/L)_{eq}$*=34*.

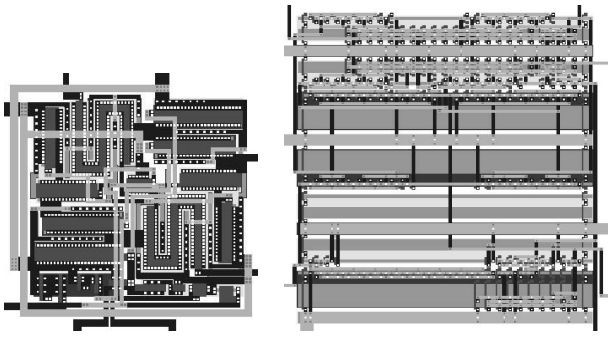

Figure 4: OTA folded-cascode layout: (a) Full-custom and (b) on SOT array.

The electrical parameter characterization is even poorer for low-voltage biasing of the transistors, which explains further discrepancies observed when using the digital technology parameters. The foundry-supplied Spice models do not reflect accurately the analog behaviour for low amplitude DC signal, which will require further in-house characterization work. This is one of several challenges to be addressed in the low-voltage operation of analog circuits in a digital technology. The full-custom had centroid positioned input pairs of 5.0μm channel length. The SOT implementation, on its turn, achieves good matching by averaging over the dozens of transistors needed to implement a single schematic-level transistor.

The SOT folded-cascode amplifier had 4db less gain when compared to its full-custom implementation, while having half the offset voltage, due to the averaging behaviour of the association with respect to random *W/L* and V_t variations.

Measured data of Table 1 are the average for the measurements on 9 samples of the OTA folded-cascode SOT. The load capacitance (C_L) values of the Table 1 were calculated from output current (I_{estim}) estimated and determined with simulated slew-rate (*SR*) and load capacitance used in a simulation. The GBW product is 3 times larger for the SOT design, at same slew-rate.

	Simulation		Measurement	
	Full-cust	SOT	Full-cust	SOT
A_V (db)	106	90.8	64.5	62.9
GBW(MHz)	4.5	6.4	0.60	2.17
V_{os}(mV)	-	-	+30	-15
SR (V/μs) @ C_L(pF)	2.9 10	10.7 5	1.51 19.2	1.47 36.4
PM (^{o})	76	63	79.4	51.7
$V_{o\ max}$(V)	+2.2/-1.3	+1.6/-1.4	+1.1/-0.7	+0.9/-0.9

Table 1: OTA's measured performance.

4. Conclusions

Despite the predictable SOT array limitations for analog circuits as a pre-diffused architecture, the performance of analog-digital mixed circuits on SOT array is satisfactory without major penalties, being comparable to full-custom. Our experimental results warrant the direction of work towards better models for digital transistors, as well as manifest *a priori* the validity of the development of SOT analog circuits based on the composite trapezoidal transistor approach. Comparing the full-custom to the SOT array design methodologies, both reached similar performance. The need for different types of transistor geometry not available in the SOT array can be overcome with adequate techniques demonstrated previously. The SOT array presents expected natural limitations as a pre-diffused architecture with no analog support.

References

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