SOI Digital CMOS VLSI - A Design Perspective

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Abstract—**This paper reviews the recent advances of SOI for digital CMOS VLSI applications with particular emphasis on the design issues and advantages resulting from the unique SOI device structure. The technology/device requirements and design issues/challenges for high-performance, general-purpose microprocessor applications are differentiated with respect to low-power portable applications. Particular emphases are placed on the impact of floating-body in partially-depleted devices on the circuit operation, stability, and functionality. Unique SOI design aspects such as parasitic bipolar effect and hysteretic V_T variation are addressed. Circuit techniques to improve the noise immunity and global design issues are discussed.**

1. INTRODUCTION

Silicon-on-insulator (SOI) technology has long been used in radiation-hardened and high-voltage applications. In the past few years, due to the impressive progress in materials, process/device, and product research/development, SOI technology has emerged as a strong contender for low-power portable applications. It is only until very recent years, however, that SOI has been seriously considered for mainstream high-performance general-purpose microprocessor applications [1, 2]. The ever-demanding performance of general-purpose microprocessor dictates far more stringent technology/device requirements and poses much more complicated design issues/challenges compared with low-power portable applications. The underlying reasons and the resulting divergence in the technology/device choice/design are discussed, and the design issues differentiated. We then focus on the impact of floating-body in partially-depleted devices on the circuit operation, stability, and functionality. Unique SOI design aspects such as parasitic bipolar effect and hysteretic V_T variation, and circuit techniques to improve the noise immunity are addressed, as are global design issues.

2. SOI TECHNOLOGY AND DEVICE CHOICE

The slow appearance of SOI in mainstream digital CMOS applications is primarily due to the rapid progress and scaling of bulk CMOS technology. As the scaling of the bulk CMOS approaches the end of the roadmap (0.12 μm - 0.07 μm), the technology evolution decelerates to a slower pace, and SOI stands a better chance of becoming the mainstream technology than before [1]. Beyond the limit of bulk CMOS scaling (50 nm - 25 nm), thin-body SOI (Fig. 1(a)) [3] and dual-gate SOI (Fig. 1(b)) [4] hold the promise to be the "future" technology/device choices. In order to suppress the off-state leakage in these devices, the silicon film thickness should be thinner than 1/4 of the channel length [5]. To overcome the large source/drain series resistance and the very low V_T (with thin gate oxide) due to the thin silicon film, raised (or thick fan-out) source/drain structures are employed and the desired V_T is achieved through gate work-function engineering (by adjusting the composition of a poly-SiGe gate) [3]. The dual-gate SOI device has all the benefit of the thin-body SOI device plus two times the current drive. The top and bottom gates must be perfectly aligned to each other and to the source/drain doping and fan-out, as mis-alignment will cause extra gate to source/drain overlap capacitance and loss of current drive [4]. These devices are "ideal" from designers' point of view since there is no circuit/design issue or complication (except the layout of the dual-gate device). They, however, pose tremendous challenges on technology development and manufacture.

At present and in the near future, the primary SOI technolgy/device choice is between a fully-depleted (FD) device (Fig. 1(c)) and partially-depleted (PD) device (Fig. 1(d)). In a fully-depleted device, ultra-thin (< 50 nm or so) silicon film is used so the depletion layer extends through the entire film. Use of fully-depleted device significantly reduces the floating-body effect. However, its large source/drain series resistance limits the performance. The process and device design are less compatible with the bulk CMOS. Its very low device V_T with thin gate-oxide and large sensitivity to process and thickness variations pose manufacturability concern and scalability limit. Partially-depleted device, with film thickness around 150 nm, alleviates the constraint on the source/drain series resistance and V_T, offering higher performance and easing the manufacturing problem by allowing the doping profiles to be tailored for any desired V_T. The process and device design are also much more compatible with the bulk CMOS [6, 7, 8]. However,the floating body in partially-depleted device, and the resulting parasitic bipolar effect and hysteretic V_T variation represent serious design issues/challenges for circuit designers [2].

3. LOW-POWER APPLICATIONS

For low-power portable applications, power and cost are the primary considerations. There is less demand on performance and scalability, thus no need to use the most advanced technology. The transistor count is low, thus manufacturability and design resource are of less concern. The low-voltage operation alleviates the reliability issues and suppresses the parasitic bipolar effect. Highly regular circuit structures, such as the MAC (Multiply-Accumulate-Cell) in DSP applications, result in less demand on design methodology and resource. The choice of technology/device (fully-depleted vs partially-depleted) is less crucial. For these applications, decision to use the fully-depleted device tends to be based on its ease of design. When partially-depleted device is chosen, body contacts (for rail-tie to suppress the floating body effect or for smart body contacts to dynamically control the threshold voltage) can be easily incorporated since there is much less area constraint. The operating frequency is low, so body contacts are easily effective. These application-specific features result in the prolific use of smart body contacts in CPL and SIMOX-MTCMOS type of circuits for deep sub-1.0 V applications [9, 10].

4. HIGH-PERFORMANCE APPLICATIONS

High-performance general-purpose microprocessor applications place ultimate demand on performance and scalability. The state-of-the-art microprocessors contain tens to hundreds of millions of transistors. The performance requirement and considerations for manufacturability, scalability, and compatibility with the bulk CMOS device design and process strongly favor the partially-depleted device [11, 12]. On the other hand, circuit designers are forced to face the design complexity resulting from the floating-body. Wide variety of circuits (from static, dynamic, pass-transistor based, to self-timed circuits) and design style (from full-custom, semi-custom, to synthesis) are employed in these microprocessors. Because of the area limitation, the use of body contacts have to be highly selective. Furthermore, for the body contact to be effective at the high operating frequency, low RC time constant is essential, yet difficult to achieve under the process/device constraints [2]. Smart body contacts, if ever intended, are containable only in drivers, arrays, and some highly regular structures. Global use of smart body contacts require sophisticated tool capability/development. Designs with floating body and/or smart body contact require detailed circuit characterization different from the bulk-CMOS. Layouts with body contacts are incompatible with bulk-CMOS. Circuit simulation with floating body requires substantially more memory and simulation time. The problem is aggravated by the long time for the DC convergence of the initial solutions and the prohibitively long time to reach steady-state for large scale circuits. The timing methodology is complicated by the topology and history/pattern dependency. In the state-of-the-art high-performance microprocessor, about 40-50% of the required on-chip decoupling capacitance is supplied by the "built-in" non-switching capacitances such as the diffusion-to-well and well-to-substrate capacitance. In SOI technology, with the faster circuit speed and absence of these "built-in" decoupling capacitances, the supply and ground bounce is more severe [2]. Finally, floating-body induced noise and globally-coupled noise have to be properly accounted for in the noise and checking methodology.

The first demonstration of a SOI microprocessor was the porting of the "core" of DEC StrongArm-110 (with phase-locked loop and ESD protection circuits disabled) for embedded applications to a 2.0 V 0.35 μm partially-depleted SOI technology reported in December 1997 [13, 14]. A compact Schottky body-contact scheme (Fig. 2), where a Schottky diode between the source/drain and body was formed wherever the source/drain implant into the silicided source/drain region was selectively not performed, was employed to suppress the floating-body effect. The result demonstrated over 20% performance improvement over the bulk CMOS at the same V_{DD} or 50% reduction in power at the same operating frequency. In February 1999, a 600 MHz, 14 W 64b ALPHA microprocessor was demonstrated in a 0.25 μm 1.5(Int.)/2.5(Ext.) V fully-depleted SOI technology based on a 433 MHz, 25 W design in 0.35 μm 2.0(Int.)/3.3(Ext.) V bulk CMOS technology [15]. As fully-depleted technology was chosen, the porting to the SOI technology was relatively straightforward. Also reported at the same time were two SOI PowerPC microprocessors: a 580 MHz 32b PowerPC-750 (based on a 480 MHz bulk CMOS design) [11] and a 550 MHz 64b PowerPC microprocessor (based on a 450 MHz bulk CMOS design) [12], both in a 0.12 μm L_{eff} partially-depleted SOI technology with Cu interconnect.

5. PARASITIC BIPOLAR EFFECT

Certain circuit topologies and switching patterns are susceptible to the parasitic bipolar effect, and logic state error can occur if the effect is not properly accounted for. Examples are: (1) stack OR-AND-like structure (e.g. dynamic OR, Fig. 3), (2) pass-transistor based design (e.g. wide multiplexer and pseudo 2-phase dynamic logic circuit), and (3) multi-level voltage-switch current-steering circuit (e.g. dynamic CVSL XOR circuit) [16, 17]. The topology typically involves a "off" transistor situated high in a stack or in pass-gate configuration, with the source and drain voltage set up in the "High" state (hence the body voltage at "High". When the source is subsequently pulled down either by the clocked evaluation transistor (in dynamic circuit) or by the input signal (in pass-gate configuration), large overdrive is developed across the body-source junction, causing bipolar current to flow through the lateral parasitic bipolar transistor. The parasitic bipolar current and the FET current (caused by noise and aggravated by the lower V_T) result in a loss of charge on the precharge (or dynamic) node. This has been shown to cause failure in a dynamic adder circuit (Fig. 4) in a 580 MHz RISC microprocessor (PowerPC 750) in a 0.12 μm L_{eff} SOI technology with Cu interconnect [11]. One can size up the keeper device (at the expense of few % in performance) or selectively dropping body contacts (at the expense of few % in area) to overcome the effect. Alternative implementation of a given function and circuit techniques have been used to improve the noise immunity of dynamic circuits on SOI with minimal impact on their delays [12]. These approaches exploit the reduced charge sharing effect and reduced delay dependency on stack ordering in SOI technology. Examples are: (1) "pre-discharging" technique (Fig. 5) that discharges intermediate nodes in a stack so bodies of the transistors high in the stack are prevented from charging to a high potential, (2) "re-arrange the pull-down tree" to position the widest parallel group of transistors at the bottom of the stack, (3) "re-ordering (cross-connecting) inputs" in multiple-fingered stacked transistors such that the signal connecting to the gate of the higher transistor in one stack connects to the lower transistor in the other stack, thus preventing one-half of the transistors from conducting parasitic bipolar current, (4) "early discharge" to force parasitic bipolar current to occur during the precharge phase, (5) "re-mapping" boolean logic to reduce the parallel stacks, (6) "complex domino" structures with the output inverter replaced by a static NAND or NOR gate to break up large parallel logic trees. During stress testing, "conditional" feedback, where a additional feedback half-latch is conditionally gated by the test signal, can be used to enhance the noise immunity. These techniques have been used to achieve robust operation in a 550 MHz 64b PowerPC microprocessor in a 0.12 μm L_{eff} SOI technology [12].

In well-designed state-of-the-art devices, the parasitic bipo-

lar leakage can be suppressed to well below 10 μA/μm [6, 7]. Experimentally, the parasitic bipolar effect does not appear to increase as the channel length (hence "base width" of the parasitic bipolar transistor) is reduced since the transistor structure- and doping-wise is far from an ideal bipolar transistor. The effect decreases significantly with scaled supply.

6. HYSTERETIC V_T VARIATION

Due to the long time constants for various body charging/discharging mechanisms (impact ionization current and junction leakage/current), the body potential during the switching transient is determined primarily by the external biasing and capacitive coupling. Depending on the circuit topology, process/device design details, and the relative magnitude of the various charging/discharging mechanisms, the body may gain or lose charges through the switching cycle, causing the body voltage to drift until steady-state is reached. The hysteresis has been known to result in frequency-dependent delay variation and shown to cause pulses to stretch or shrink [18, 19] as they propagate down an inverter chain. Since the majority of CMOS circuits are inverting-logic, the effect is pervasive.

The hysteretic delay variations of a basic static inverter in a $L_{eff} = 0.145\,\mu$m PD/SOI technology are illustrated in Fig. 6(a), where the output-rise-delay (TD_{rise}), output-fall-delay (TD_{fall}), and average delay (TD_{ave}, average of TD_{rise} and TD_{fall}) are shown as functions of time when the inverter is continuously cycled at 50% duty cycle with $V_{DD} = 1.8$ V and T = 27 °C [20]. Two cases are shown, corresponding to two different initial states (input at "Low" or "High" for a sustained period of time) for the circuit. The body-to-source voltages of the nMOS and pMOS device through the switching cycles are shown in Fig. 6(b). Notice that different initial states result in delay disparity at beginning of the switching activity, yet converge as the circuit approached the steady-state (since the steady-state is determined only by the net charges gained/lost through the switching cycle and is reached when the net charges gained/lost through the switching cycle equal to zero). A detailed study of the dependence of the hysteretic gate delay on the supply voltage, W_p/W_n ratio, duty cycle, slew rate, output load, and initial state of the circuit is presented in Ref. [20].

Pass-transistor based circuits and circuits using stacked transistors are known to be of high performance leverage in SOI due to the lack of reverse-body effect [2]. These "high-leverage" circuits, however, tend to exhibit highly-hysteretic behavior. The performance leverage comes about because the body is rarely reverse-biased (and actually tends to be forward-biased) with respect to the source. Since there are always biasing conditions or switching patterns that reduce the forward-bias of the body/source junction, the performance leverage comes hand-in-hand with large hysteretic delay variations. This is exemplified by the single-ended CPL circuit (known as LEAP) shown in Fig. 7(a) [21], where the pass-transistor qA is initially set up with both its input (IN1) and output at "High" (thus its body at V_{DD}), and its gate select signal (A) at "Low". The gate select signal A then switches to "High", and the data input $IN1$ is subsequently pulled down. As the gate select signal A switches "High", the body voltage of nMOS qA is capacitively coupled up. With both the source and drain of transistor qA at V_{DD}, the inversion layer in the channel never forms, and the capacitive coupling between gate and the body is very strong through the entire gate signal ramping. The body voltage is thus boosted to 2.44 V, significantly above V_{DD} (1.8 V), resulting in fast first switch. Fig. 7(b) shows the variation of body voltage and delays for "rising input" transition as functions of time, and with the frequency as a parameter. The period for which IN1 signal is "Low" remains constant at 1.0 ns in every switching cycle. Hence higher frequency (higher duty cycle) implies shorter duration for which input $IN1$ remains "High", and thus less time for the body to get charged (by the reversed-biased drain-to-body and source-to-body PN junction current, noting that both drain and source will be at V_{DD} after input $IN1$ rises). This effect can be clearly seen in Fig. 7(b), where the body voltage falls much faster when IN1 is switching at 500 MHz compared with the case when IN1 is switching at 50 MHz or 5 MHz. The hysteretic variation is particularly significant for the "rising input" delay due to the V_T loss in passing the "High" state. The "rising input" delay changes from 0.90 ns at $t = 2.0$ ns to 0.130 ns at $t = 40002$ ns (a change of 44.4%). Use of dual-rail CPL with cross-coupled pMOS load (Fig. 8(a)) significantly reduces the delay variation (Fig. 8(b)) and its frequency dependence [21]. This is because the "falling" transition through the nMOS tree helps the rising transition of the complimentary nMOS tree through the cross-coupled pMOS. Thus, the "rising input" delay and its variation are compensated by the "falling input" of the other branch.

The hysteretic V_T variation affects the duty cycle and degrades the clock skew and jitter in clock distribution network [2]. The clock distribution network typically consists of multiple level of trees/buffers, so the effect is cumulative. Extra "guard band" is necessary to absorb the delay variations in clocks and latches, and to protect against early mode (or race condition). If "gated clock" is used, additional margin is required to properly account for the variations in clock duty cycle, skew, and path-delay between the first switch (when the clock first becomes active) and the steady-state (when the clock is continuously running). Similarly, margins have to be widened to account for transitions from "low power mode" (where the entire global clock distribution or portion of it is shut down) and "test mode" (where the system clock is stopped, and test clocks at much lower frequency are used to scan-in/scan-out test patterns) to normal operating mode [11]. In the 580 MHz PowerPC 750 SOI microprocessor, the latch hold-times were increased by 25-40 ps to protect against early-mode. Latch race margins were increased by another 5.0 ps to account for additional skew in local clock generation. Margin of 25 ps is added to half-cycle paths between globally gated latches for transition from low power mode to normal mode, and 25 ps race margin budgeted for latches interfacing between the globally gated and ungated clock domains. Many short-path margin were increased to overcome variations in path delays [11].

The hysteresis effect complicates the timing methodology, degrades the timing rules, and complicates the design and

degrades the margin of self-timed type of circuits widely used in the stat-of-the-art on-chip cache SRAM [2]. Fig. 9 illustrates the situation where the race condition between a self-timed path (which fires every cycle) and a pull-down discharge path (which starts "fresh" after a long period of "no discharge"), causes a failure in the PowerPC 750 SOI microprocessor [11]. The self-timed path was slowed down to overcome this problem.

As the supply voltage is scaled, the impact ionization current decreases. Scaled device design for lower supply voltage also tends to alleviate the hysteretic V_T variation [22]. However, the balance point between the body-to-source forward junction current and the drain-to-body reverse junction leakage, which determines the body potential at DC equilibrium, is relatively independent of V_{DD} due to the weak dependence of the reverse junction leakage on V_{DD}. Furthermore, variation in V_T becomes a larger portion of the total supply voltage. The hysteretic V_T variation, therefore, remains a serious design concern/challenge even at low supply voltage.

7. CACHE SRAM

SOI technology has been known to improve the soft error rate (SER) and reduce the bitline capacitance. Due to the buried oxide in SOI MOSFET, appreciable charge collection can only occur when an α-particle hits the channel region. Although the amount of α-generated charges in SOI MOSFET is substantially less than that in a bulk MOSFET, the total charges collected at the cell storage (drain) node can be significantly higher than the α-generated charges due to the parasitic bipolar effect. Detailed 3-D simulations shows that the α-induced bipolar current flows over a long period [23]. SER measurement on a 0.35 μm 256-Kb SOI SRAM with a 128-Kb block in 28 μm^2 floating-body cell and the other 128-Kb block in 42 μm^2 body-tied cell showed that the SER of the floating-body cell was about 300 times worse than the body-tied cell. Hence, in order to maintain the superior SER of SOI SRAM, it is essential to reduce the parasitic bipolar effect [24].

The cell size and performance of SOI SRAM can be improved by using a cell layout with abutted n^+ and p^+ drain regions [25]. In 0.35 μm design rules, a cell size reduction of 16%, bitline capacitance reduction of 39%, and access time improvement of 10-20% have been demonstrated in a 128-Kb SRAM macro compared with the bulk counterpart. Other factors, such as scaled groundrules, local interconnect and wiring limitations, SER considerations, and the use of phase-shifting lithography at selected levels, may result in additional rules, thus prohibiting one from realizing the full cell size advantage.

For SRAM, the primary concerns due to the floating body are the bit-line capacitance disparity, bit-line leakage during read operation, half-selected cell disturb during write operation, and the sense transistor V_T mismatch [2, 12]. In general, body contacts should be used in the sense transistors to improve the sense margin. Repetitive reads of one data state in a bit-column can cause offsets in the body voltages, resulting in sense transistor V_T mismatch. The mismatch can cause up to 100 mV sense-amp offset under extreme conditions, resulting in failure when the sense-amp signal develops too quick. The problem is typically addressed by the use of body contacts or by increasing the sense delay to allow a sufficient bit-line differential voltage to develop slowly [2, 11].

8. CONCLUSION

We have reviewed the design considerations for SOI digital CMOS VLSI. It was shown that the ever-demanding performance of general-purpose microprocessor dictated far more stringent technology/device requirements and posed much more complicated design issues/challenges compared with low-power portable applications. Unique SOI design aspects resulting from the floating-body in partially-depleted devices, such as parasitic bipolar effect and hysteretic V_T variation, were discussed. Circuit topologies susceptible to parasitic bipolar effect and circuit techniques to improve the noise immunity were addressed. The impact of hysteretic V_T variation on various circuits (static CMOS, CPL, self-timed), clock distribution, latch timing, and global timing methodology were discussed. Timing large-scale logic circuits with all the floating-body related effects represents the single most-challenging task in bringing SOI into mainstream microprocessor applications. It is crucial for circuit designers to understand and quantify/contain the hysteretic delay and noise margin variations to fully exploit the performance leverage of a scaled PD/SOI technology.

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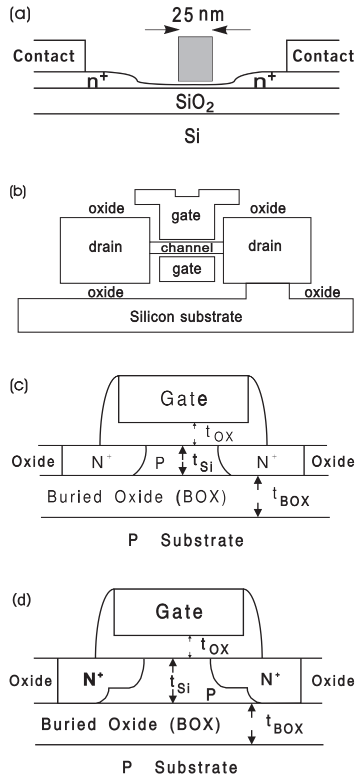

Fig. 1: Schematic cross-section of (a) thin-body SOI device ($t_{Si} < 1/4$ of L_{Gate}) [3], (b) dual-gate SOI device ($t_{Si} < 1/4$ of L_{Gate}) [4], (c) fully-depleted SOI device ($t_{Si} < 50$ nm), and (d) partially-depleted SOI device ($t_{Si} \approx 150$ nm).

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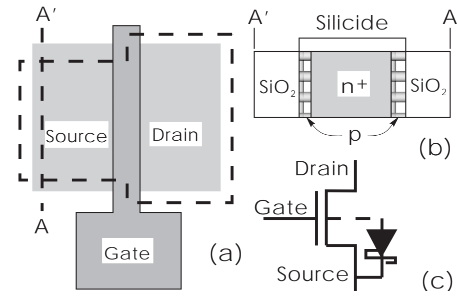


Fig. 2: PD-SOI nMOS with Schottky body-contact at source: (a) top view, dashed line indicates N^+ source/drain implant mask, (b) source cross-sectional view, and (c) device schematic. (Ref. [13, 14]).

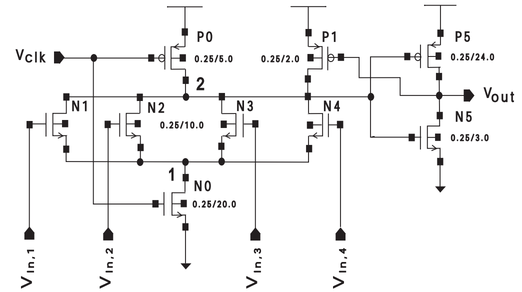


Fig. 3: A dynamic 4-way OR circuit. For some conditions, parasitic bipolar current can flow through the "off" logic transistors, discharging the dynamic node [16].

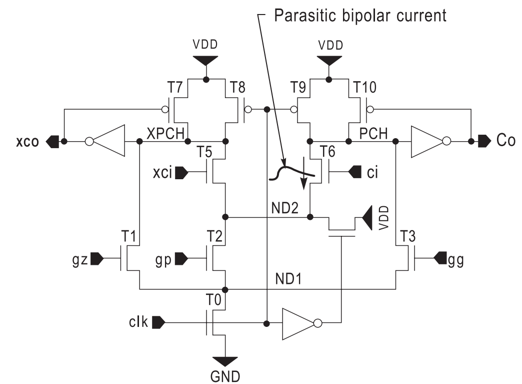


Fig. 4: A dynamic carry look-ahead adder circuit, where the parasitic bipolar current discharges the dynamic node to cause a failure [11].

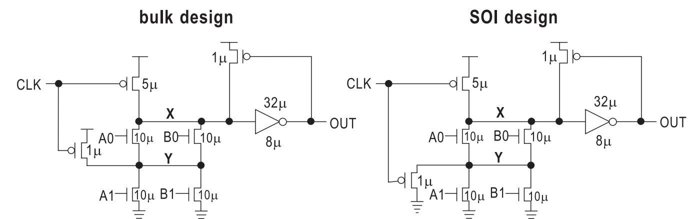


Fig. 5: Pre-discharge technique. In "bulk design", intermediate nodes (Y) in a stack are precharged to V_{DD} in precharge clock phase to minimize charge sharing. In "SOI design". intermediate nodes are "discharged" in precharge phase to prevent parasitic bipolar effect [12].

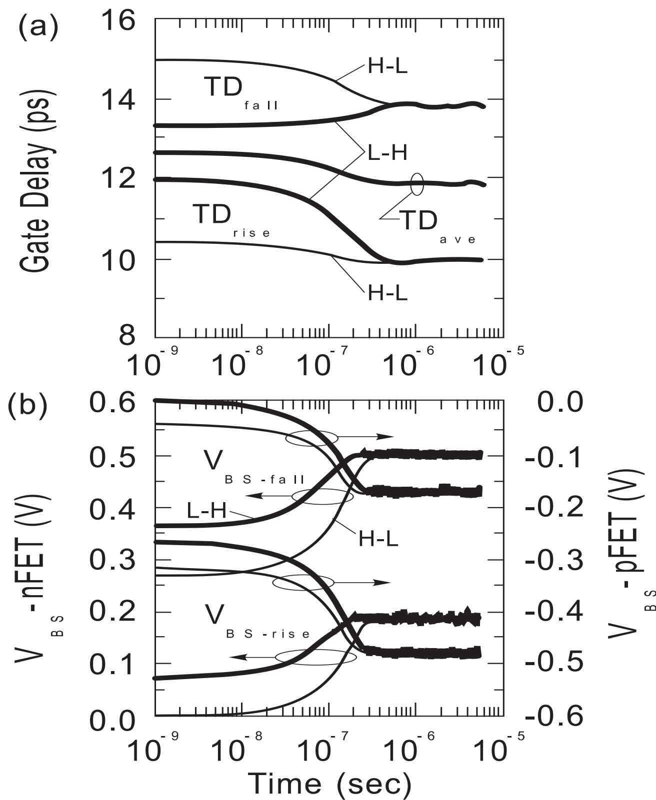


Fig. 6: Hysteretic delay variation for a static CMOS inverter: (a) TD_{rise}, TD_{fall}, and TD_{ave} as functions of time, and (b) body-to-source voltage of nMOS and pMOS as functions of time. (W_p/W_n = 2, 1.0 ns period, 50% duty cycle, initial input at "Low" (L-H), and initial input at "High" (H-L)) [20].

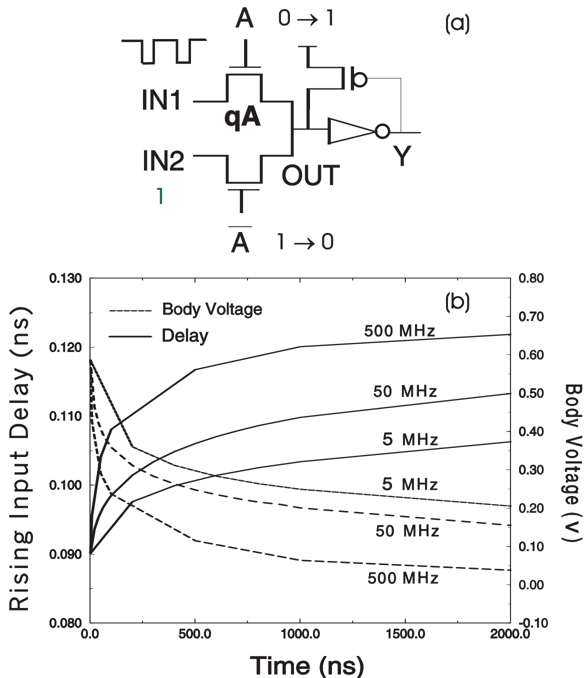
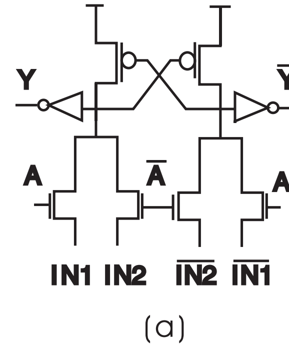


Fig. 7: (a) A single-ended LEAP circuit, and (b) variation of body voltage and delay as functions of time for "rising input" with input pulse frequency as a parameter in a 1.8 V, L_{eff} = 0.12 μm PD/SOI technology. (Input pulse width fixed at 1.0 ns) [21].



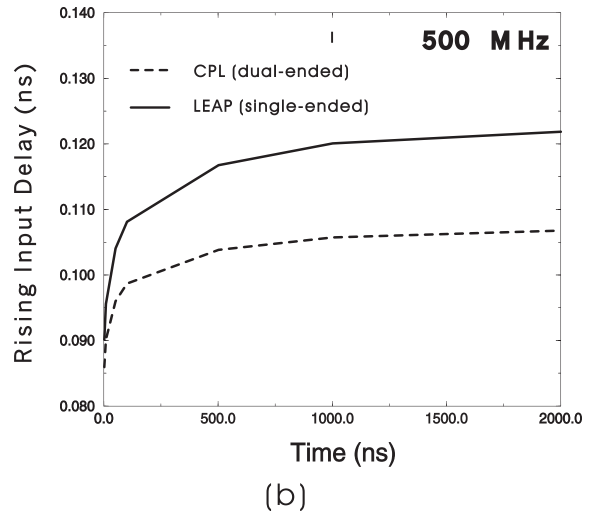


Fig. 8: (a) A dual-ended CPL circuit, and (b) comparison of "rising input" delay variation with time for CPL and LEAP circuit in a 1.8 V, L_{eff} = 0.12 μm PD/SOI technology [21].

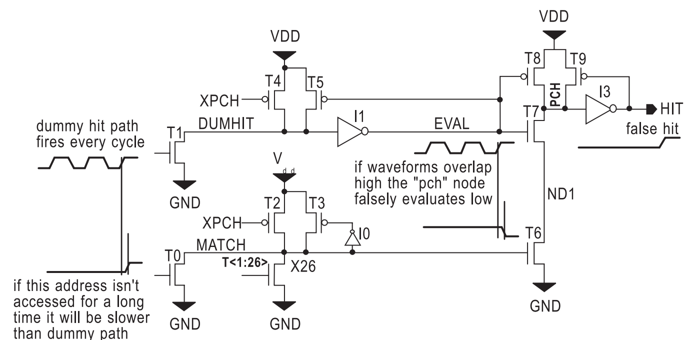


Fig. 9: A 27b dynamic OR with self-timed mask. Hysteretic V_T variation causes race condition between the self-timed path and the pull-down discharge path [11].