Design and Optimization of Power/Ground Network for Cell-Based VLSIs with Macro Cells

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Abstract: This paper deals with the design and optimization of mesh-based power/ground network for cell-based VLSIs with macro cells. These macro cells absorb a lot of current, furthermore, the current that each pin of the macro cell absorbs is not known, which introduces a new problem to the design of power routing. This problem hasn't been discussed so far. In this paper, a new algorithm is presented to solve this problem. The algorithm includes 3 sub-algorithms: searching feasible solution, cutting branches and minimizing strap width. The algorithm has achieved the object which minimize the area of power straps with high running speed.

Key words: Power, Cell-Based VLSIs, Optimization, Mesh, Macro Cell, Branch-and-Bound

1. Introduction

Power and ground (p/g) distribution is always very important in the design of VLSIs because p/g nets cover a large portion of chip area. So it's often given the first priority in routing process. There are two basic problems in the design and optimization of p/g nets. The first is the undesirable wear-out of metal wiring caused by electromigration, and the second is the narrowing margins caused by voltage drops. Increasing wire width can solve these problems. However, it is too expensive to use the wiring resource freely. Consequently, it is necessary to minimize the area p/g nets used.

Generally speaking, p/g nets design consists of two main tasks. Firstly, a topology, which can be trees[1] and meshes[2]-[6], is constructed. Secondly, the area of p/g nets is minimized. Many studies on p/g design have been published, but most of them assumed single-layer routing without the use of vias and only single power supply pad is available. However, with the recent progress of technology, the routing can be done in 3 to 5 layers. Those conventional methods for p/g nets design are not suitable to modern cell-based design.

As Figure 1 shows, the p/g nets of cell-based VLSIs include mandatory wiring including peripheral power buses, power pads, basic rows and power rails. Mandatory wiring is predetermined by its die size and chip architecture. The wiring width of power rails is fixed. Recently, power enhancement straps as figure 1 shows are used to improve reliability and quality of power supply because of the increasing of VLSI scale. At first enhancement power straps are added manually by chip designers. There is no theoretical basis for the addition of these straps, and also they will consume many wiring resources.

How to add these straps and minimize their area hadn't been discussed until Takashi and Kuh presented a method[6] to optimize p/g nets for cell-based VLSIs. They assume the topology is fixed and only minimize the strap width by

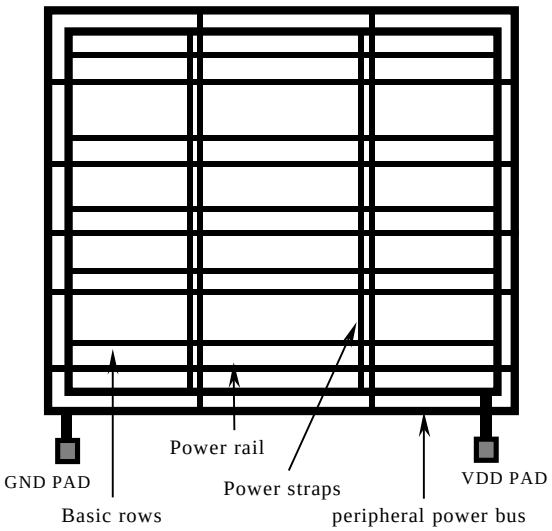

Figure 1: Mesh-Based Network

Feasible direction method, but it has some disadvantages: 1) The p/g topology is not optimized. 2) It consumes a great deal of running time and memory. 3) After the optimization, it has a solution in floating point domain, and maybe there is no feasible solution in integer domain. To overcome these disadvantages, we had presented a method[7] to do the topology optimization and width optimization at the same time and get good results for cell-based VLSIs.

However, cell-based VLSIs often contain some macro cells, which absorb much more current than small ones, so it's a big problem to supply the current to macro cells without the violation of circuit constraints. Obviously, the sum of the current which macro cells absorb is known. If the absorbing current of macro cell's pins is known, we can still use algorithm[7] to design and optimize p/g nets with only small changes; otherwise, the problem is difficult to solve because the p/g nets should meet all cases no matter what the absorbing current of the macro cell's pins are. It seems that there is no method presented to deal with this case up to now.

In this paper, an efficient algorithm is proposed to solve this problem. Our algorithm has 3 steps. At first, it can find a topology that has the minimal number of straps by the method of branch-and-bound without violating the constraints, then some of the strap branches will be cut, at last the width of the straps is minimized.

2. Mesh-Based Power and Ground Network Model With Macro Cells

To supply the current to macro cell, we place a power

ring around it. The pins of macro cell connect to power ring, through which the pins absorb current. The width and location of power ring is also fixed. The power rails and straps connect to the power ring as Figure 2 shows.

Figure 3 shows the equivalent circuit of the power and

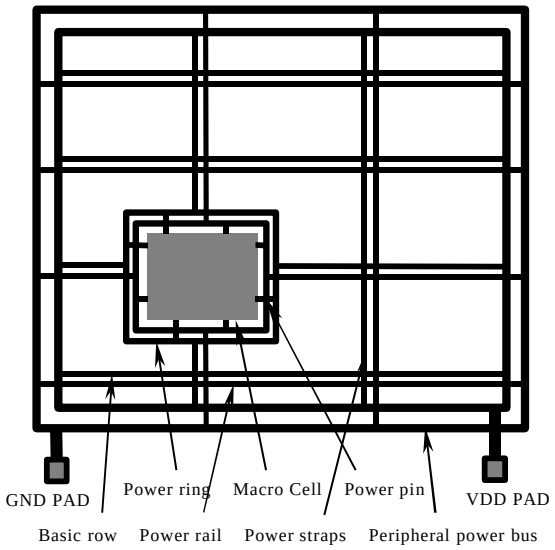

Figure 2: Mesh-Based Network with Ring

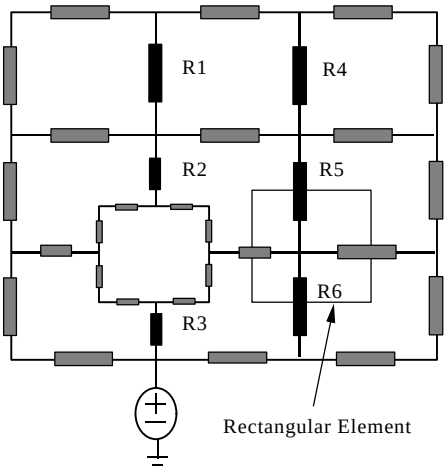

Figure 3. Equivalent circuit of power supply

ground network. The nodes on the power ring around macro cell can be divided into two types. The first type is the node which absorbs the current. These nodes are the points at which the pins of macro cell connect to the power ring. The second type is the node which connect to power rails and power straps. For simplicity, we only consider power nets in this paper, and the ground is the same as the power.

3. Problem Formulation

In order to formulate the problem, we first have the following definitions:

N_n : Set of all nodes.
N_b : Set of all branches.
E_s : Set of all power enhancement strap edges.
N_{re} : Set of leaf nodes.
W_i : Width of branch $i \in N_b$.
L_i : Length of branch $i \in N_b$.
I_i : Current in branch $i \in N_b$.
R_i : Resistance of branch $i \in N_b$.

In this paper, we define J as maximum current density, r as sheet resistance and ΔV as maximum voltage drop. All nodes are divided into 4 kinds: ***supply node*** is power pad; the nodes which absorbs current are called a ***leaf node***, the node which is connect to the pin of macro cell is defined as a ***ring node***. For other nodes, we call them ***medium node***. Given a cell placement, we can model the p/g nets according to Figure2. The routing problem can be formulated as follows:

Objective Function : Our goal is to minimize the wiring resources which the power enhancement straps used. Thus objective function can be defined as the area of the power straps.

$$Z = \sum_{i \in E_s} W_i L_i$$

Voltage Drop Constraints : In this paper, we only consider vertical voltage drop constraints which can include the horizontal voltage drop constraints in most cases according to [1]. So the voltage drop constraints can be represented as below:

$$\sum_{j \in path(pt,i)} I_i R_i \le \Delta V \qquad i \in N_{re}$$

pt is one of the power pad nodes, *path (pt, i)* represents the whole path between node *pt* and *i*.

Electromigration Constraints : For all the branches in the circuit, the maximum current constraints due to electromigration are determined as follows:

$$I_i \le J \quad i \in N_b$$

Circuits Constraints : The power and ground routing should also obey *Kirchhoff's* current law *(KCL)* and voltage law *(KVL)*. In this paper, we use the node voltage equation set to represent *Kirchhoff's* law. In this equation set, we assume the node voltages as the variables and the current of the branches can be calculated from its two connected node voltages. For all branches we also have *Ohm's* law as follows:

$$V_i = I_i R_i \qquad i \in N_b$$

Power Ring Constraints : **T**he node voltage equation set mentioned above is not full rank because we only know the current sum macro cell consumes and the current each pin of the macro cell absorbs is unknown. So the power ring constraints are defined as the set *Q*:

$$Q = \{(I_1, \cdots, I_k, \cdots, I_{N_{ring}}) \mid \sum_{k=1}^{Nvertex} I_k = I_{ring}, I_k \in [0, I_{ring}]\}$$

where I_{ring} is the current sum of macro cell; I_k is the current which the kth pin of macro cell absorb; *Nvertex* is the number of *Q*'s polar points. The node voltage is the variables in these equality and inequality. The set of these equality and inequality is the solution field of our problem and can be represent as follows: $S = \{V \mid GV \ge B\}$. V is the vector of node voltage. G is coefficient matrix made up by the conductance in the circuits.

4. Solution Method

Our algorithm has three steps. In each step, we ought to check a topology feasible or unfeasible. A feasible topology doesn't violate the constraints no matter what the current distribution of macro cell is. To solve this problem

we first build the theoretical basis of our algorithm.

4.1 Theoretical Basis

The solution field in this problem is $S=\{V \mid GV \geq B\}$. Obviously, *S* is a linear system, which is a convex set. Similarly, *Q* is a bounded convex set too. We present a theorem as below:

Inclusive Theorem : Set *S* is a convex set, *Q* is a bounded convex set which has the finite polar points $I^{(1)}, I^{(2)}, \cdots, I^{(Nvertex)}$, *Nvertex* is the number of *Q*'s polar points, then

$$I^{(1)}, I^{(2)}, \cdots, I^{(Nvertex)} \in S \quad \Rightarrow \quad Q \subseteq S$$

Since *Q* is a bounded convex set, it has the finite polar points $I^{(1)}, I^{(2)}, \cdots, I^{(Nvertex)}$. Each element of *Q* can be represented by a certain convex combination of *Q*'s polar points according to ***Representation Theorem***[8] as follows:

$$I = \sum_{j=1}^{Nvettex} \lambda_j I^{(j)} \quad \lambda_j \geq 0 \quad j = 1,2,\cdots, Nvertex$$

Because all the polar points of *Q* are in the set *S* as we set, each element of *Q* can be represented by a convex combinations of some elements of *S*. For *S* is a convex set, we can prove that $Q \subseteq S$ due to the definition of convex set.

This conclusion can be illustrated in 2 dimension as the Figure 4 shows. The polar points of *Q* is *a*, *b* and *c*. If all these polar points belong to *S*, we can say that *Q* belongs to *S*.

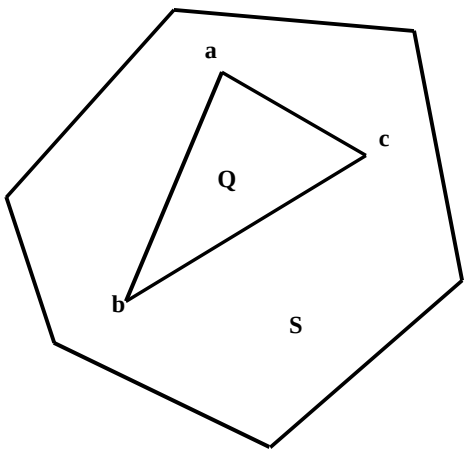

Figure 4 The case in two dimension

The next problem is how to obtain polar points of *Q*. Because *Q* is a bounded super plane, the polar points of *Q* are very simple. The kth vertex of *Q* is ($I_1 = 0$, $I_2 = 0$, $\cdots$,$I_k = Iring$, $\cdots$, $I_{Nvertex} = 0$). Therefore, when we test a topology feasible or not, we can set the absorbing current of a certain pin of macro cell as *Iring* and others as zero in turn. If all polar points of this topology do not violate the constrains, it is a feasible solution. The number of polar points equals to that of macro cell's pins which does not changed.

4.2 Feasible Topology Searching with Minimal Number of Straps

We use the method of branch-and-bound and heuristic information to search the feasible topology which has the minimal number of straps.

At the beginning of the algorithm, the boundary of branch-and-bound is set as the number of power rails of the chip, and the initial topology have no straps. We use a binary number to represent the strap topology and the digit of this number equals to the number of the straps. For example, if there are 3 strap channels, the initial topology can be represented as 000 to show that there are no straps used.

If we find a topology violates the constraints, we will test its sons. For instance, the topology 000 has 3 sons which are 100, 010, 001. When we find a feasible topology, the number of straps this topology uses becomes the new boundary. If a topology has the number of straps no less than the boundary, it will be not searched.

The searching procedure can use the method of recurrence[7] to search the feasible topology. However, recurrence consumes a great deal of time and memory. Furthermore, it is very difficult to use the heuristic information in the searching process. So in our method, we use non_recurrence instead of recurrence. At first, we build a searching chain, then insert the initial topology into this chain. If this topology violate the constraints, the sons of the current topology are inserted into the chain. We use heuristic information to decide the order in which the sons of current topology insert the chain. This inserting order determines the searching order and leads to different experimental result and running time.

In this paper we use two kinds of heuristic information. The first one is very simple and direct: because the absorbing current of macro cell is much larger than other cells, we first search the topology which has more straps intersecting with the macro cell. The second one is a little more complex: we have noticed that the constraint violations always occur near the power pads. It is because that the current which the power pads bring about will spread around them, that is to say, the closer to the power pad, the more easily the branches current violate the constraints. To disconcentrate the current around the power pad we first compute the distance from each strap of a topology to its nearest power pad, then get the average of them. The topology with the small average will be searched earlier. The method which uses the second heuristic information has the better result than the first one.

By the method of branch-and-bound and heuristic information we can not only assure to find the feasible solution which has the minimal number of straps in the full solution field, if it exists, but also spare a lot of running time and memory.

4.3 Branch Cutting and Width Minimization

After the searching process, some of the strap branches of minimized topology can be cut under the constraints. We define a testing current and its lower bound, upper bound and the increment. First, testing current equals to lower bound. We check current topology by cutting the branches whose current is smaller than testing current. If this new topology violates constraints, current topology will remain itself and the increment is added to testing current, then new topology is checked by new testing current again; if the new topology doesn't violate the constraints, the topology will be updated by the new one and testing current come back the lower bound. This process will iterate until testing current is beyond the upper

bound of the testing current. Besides, if the number of strap branches which current is smaller than the testing current last time, the testing current will not detect this current topology and increase by the increment directly. From the experiments, this procedure can spare a lot of running time.

During the width optimization, we use dichotomy method. Upper width bound is the width of peripheral buses, and lower bound is the width of power rails. The experimental results shows the procedure of width optimization reduces the area of straps by more than ten percents.

5. Experimental Result

This algorithm has been implemented with language C(running on Sun sparc20). Using several examples, we have confirmed the validity of the problem formulation and our algorithm.

The experimental results are shown as Table 1, 2, and 3. Table 1 shows the result got by the recurrence method. Table 2 and 3 are the experimental results which uses non_recurrence and two kinds of heuristic informations respectively.

From the experimental results we can see that non_recurrence method is better than recurrence. The method which uses the second information consumes less running time than the first one.

Table 1. Experimental results got by the way of recurrence

Example	Strap number	Area of straps before cutting branches & minimizing width (μm^2)	Area of straps after cutting branches and minimizing width (μm^2)	Running time (s)
C.par	3	77120	66275	30.01
CC3.par	2	64000	54500	4.67

Table 1. Experimental results got by the first heuristic information

Example	Strap number	Area of straps before cutting branches and minimizing width (μm^2)	Area of straps after cutting branches and minimizing width (μm^2)	Running time (s)
C.par	3	77120	66275	28.37
CC3.par	2	64000	50500	4.02

Table 2. Experimental results got by the second heuristic information

Example	Strap number	Area of straps before cutting branches and minimizing width (μm^2)	Area of straps after cutting branches and minimizing width (μm^2)	Running time (s)
C.par	3	77120	66275	4.72
CC3.par	2	64000	50500	1.85

6. Conclusion

In this paper a method is proposed to design and optimize the mesh-based power network which has macro cells in cell-based VLSIs. At first we use branch-and-bound method and two kinds of heuristic informations to find a topology which has the least number of straps, then we cut some strasp branches and minimize the strap width to reduce the wring source of straps. This algorithm has obtained a good result with a very high speed. Furthermore, in the searching process, we build a searching chain which can use the heuristic information flexibly. So this algorithm can be easily extendible by using different heuristic information.

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