TITAC–2 : An asynchronous 32-bit microprocessor

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I. Introduction

With the wire-delay problem moving into dominance in VLSI chip design, a fundamental limitation is being revealed in performance and dependability of synchronous systems which require global clock distribution with as little skew as possible. The worst-case delay is influenced not only by design and fabrication process but also by the operating environment, e.g. the power supply voltage and temperature. Asynchronous systems, with no global clock, can intrinsically enjoy ; 1) average-case performance instead of worst-case performance, 2) low power consumption, 3) ease of modular design, and 4) timing fault tolerance. We have designed and implemented a 32-bit fully asynchronous microprocessor, TITAC-2, which is the fastest and largest CMOS asynchronous microprocessor that has ever been operational.

II. Architecture

TITAC-2 is a 32-bit asynchronous (clock-free) microprocessor whose architecture is based on the MIPS R2000 processor, including five-stage pipeline, on chip cache, precise exception handling, external interruption and memory protection.

Instructions are executed through 5 stages, namely, IF (Instruction Fetch), ID (Instruction Decode), EX (EXecution), ME (MEmory Access) and WB (Write Back). The pipeline structure of TITAC-2 is shown in Fig.1. The instruction set of the R2000 was modified for TITAC-2. Some R2000 instructions were not implemented, while a small number of R2000 instructions have modified operation. The modified instructions include multiple/divide, privilege instruction and delay slots of branch instructions. The object code is not compatible because of a different instruction encoding.

III. Design feature

A significant feature of the design is the introduction of a new delay model, called the Scalable-Delay-Insensitive (SDI) model, which provides with a reasonable approach to dependable and high-performance asynchronous VLSI system design.

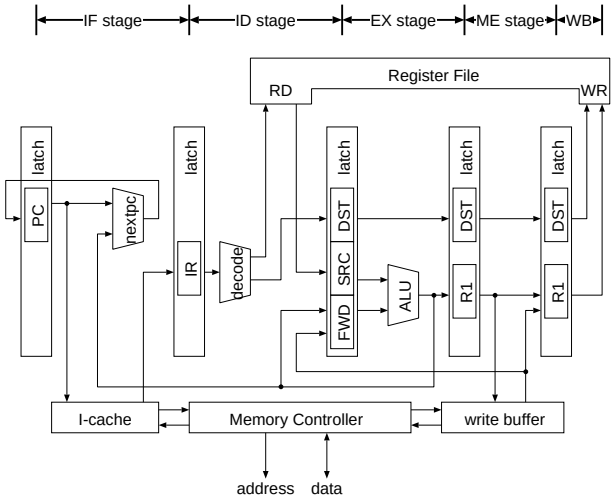

Fig. 1. The pipeline structure of TITAC–2.

The SDI model is an unbounded delay model, i.e. no upper bound is assumed on the gate and wire delays. Unlike the well-known Delay-Insensitive (DI) model, the SDI model assumes that a bound exists on the variation ratio of the relative delay between any two components. The SDI model is defined as follows;

Scalable Delay Insensitive model A component refers to a gate or an interconnection wire between two gates. Let $d1$ and $d2$ be the delay for any two components C1 and C2. The relative delay D of C1 to C2 is expressed as $D = d1/d2$. Let D_e denote the relative delay that is estimated by the designer, and D_a denote an actual relative delay observed through the system's lifetime. The relative variation ratio R is expressed as $R = D_a/D_e$. Then, the Scalable-Delay-Insensitive model assumes that the relative variation ratio R is bounded for any two components, that is, $1/K < R < K$, where K is a constant and will be called the maximum variation ratio.

An SDI circuit operates correctly even if the "actual" delay of a signal propagation path in the circuit becomes K times larger than the "estimated" delay, thus achieving a sufficient degree of delay-insensitivity, and operates much faster than the DI or Quasi-DI counterpart. In the TITAC-2 design, by taking account of the technology used, the entire system was divided into subcircuits with each subcircuit being limited within a maximum of 1.93mm $\times$ 1.93mm, which validates that the maximum variation ratio K is determined to be 2. Then, each subcircuit was designed based on the SDI model with $K = 2$, while global interconnections between subcircuits were designed based on the DI model.

IV. Asynchronous pipeline design

TITAC-2 uses two-rail four-cycle signaling for data transfer, except for the internal cache memory and external bus interface that use the bundled-data assumption. In a bundled-data system, such as the micropipelines, a special control signal with a prescribed delay element determines when bundled-data arrives. Determining an appropriate value for the delay elements is one of the most important design issues, involving a trade-off between performance and reliability. TITAC-2 accommodates presettable delay elements so that the delay value can be programmed in 0.5ns steps from outside the chip when the chip is in the reset state.

The asynchronous pipeline for TITAC-2 manages the flow of data according to the state of the next and previous pipeline stages with its control decentralized. An asynchronous FIFO(First In First Out) buffer is used for the stage latch to simplify pipeline controllers. Each stage latch contains 4 primitive latches in cascade, each of which consists of two C-elements and one NOR gate.

Our approach to the design of combinational circuits is based on the derivation of 2-rail logic implementation from Binary Decision Diagram(BDD). Transistor-level (DCVSL) implementations are used for such logic circuits that are used very frequently, e.g. adders in a multiplier, and gate-level implementations are used for other cases. In order to reduce cycle time of pipeline stage, idle phase acceleration circuit is used. That is, when a critical path of idle phase is long, AND gates are inserted at the middle point of the critical path to execute idle phase in parallel at the first half and the latter half of the AND gates.

V. Chip Implementation and Evaluation

The TITAC-2 chip has been fabricated using 3 layer metal, 0.5 micron rule CMOS standard cell technology, integrating 496,367 MOS transistors and 8.6K Byte memory macro in 12.15 mm $\times$ 12.15 mm. The first silicon of TITAC-2 runs correctly with its power supply voltage being varied through the range from 1.5 V to 6.0 V and the temperature of its package surface being heated up to about 100°C and cooled down to - 196°C with liquid nitrogen. TITAC-2 achieves 52.3 VAX MIPS using Dhrystone V2.1 benchmark consuming 2.11W at 3.3 V, 20°C. The characteristics of TITAC-2 are summarized in Table I.

Fig.2 shows the measured speed and power consumption versus power supply voltage changing from 1.5V to 4.0V at 20°C.

Table I Characteristics of TITAC-2

Process	0.5μm CMOS, 3 layer metal
Die size	12.15 mm $\times$ 12.15 mm
Transistors	496,367 + 8.6KB memory(cache)
Performance	52.3 VAX MIPS (Dhrystone V2.1)
Conditions	3.3V, 20°C
Power	2.11W

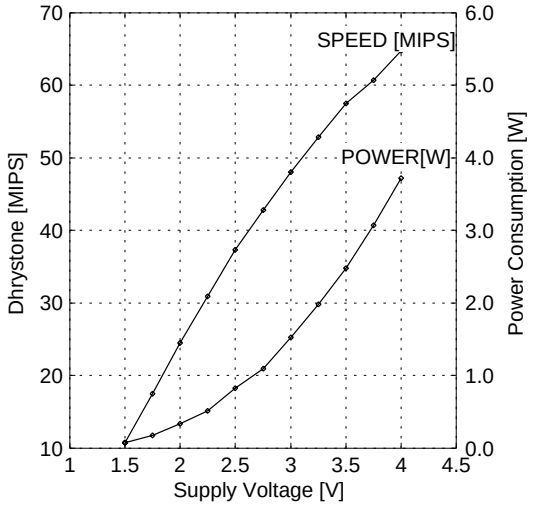

Fig. 2. Supply voltage versus speed and power consumption.

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