Inverse Modeling - A Promising Approach to Know What is Made and What should be Made

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Abstract — Inverse modeling is a promising approach to know device structures made in experiments. We show our inverse modeling approach and its efficiency by demonstrating accurate extraction of deep submicron MOSFET structures. We also show that our approach can predict device performance to optimize its structure for required specification.

I. Introduction

In order to develop deep sub-micron MOSFETs with competitive cost and reasonable turn around time, device engineers should know what they have made by split-lot experiments. This requirement seems to be trivial, but it is not so easy to precisely understand what's going on in their experimental devices. Nobody can look at real impurity profiles without destroying the devices. Even if sophisticated analyzing tools such as X-TEM, AFM, SIMS and so on are used, we can never see carrier transport behavior when the devices are operated.

Recently Technology-CAD (TCAD) tools have begun to play a quite important role to fulfill the gap between such demands and inadequate capability of the analyzing tools. Physics-based process and device simulators can show us vivid doping profiles and electron/hole distributions inside any kind of semiconductor device even under operation as well as terminal current-voltage characteristics. However, there is still a large problem to be solved in the TCAD tools. That is mainly caused by the inaccuracy of process modeling. Today's most sophisticated process simulators implement point-defect-induced impurity diffusion models, but they have a lot of fitting parameters to reproduce experimental results even in the case of one-dimensional diffusion. Moreover, those parameters are often local and cannot be applied to wide range of process conditions. As a result a process simulator output cannot reproduce experimental current voltage characteristics when it is transferred to device simulators even though the physics in device models are accurate enough to express simple devices. One promising approach to overcome the above-mentioned difficulty is so-called inverse modeling [1].

The concept of the inverse modeling is that physically precise device models can be used to determine device structures including active impurity profiles. In the case of MOSFETs C-V characteristics can be modeled only by Gauss's law-based Poisson equation that is accurately solved by a numerical method. Also, sub-threshold current voltage characteristics can be expressed by a well-known impurity concentration dependent diffusion current model. By using these C-V and I-V characteristics from experiments we can inversely solve Poisson and current continuity equations with near-equilibrium condition to obtain the doping profile and the device structure including the gate oxide thickness. Finally, self-consistent agreement of all C-V and I-V characteristics between the measurements and simulations guarantees the precision of the extracted device structure.

In this paper our much simpler approach for the inverse modeling as well as our program to support it will be described and we will show that it is used not only to know what is made in experiments but also to predictively know what should be made.

II. MOSFIT : Inverse Modeling Assist Program

Figure 1 shows the flow chart of our inverse modeling assist program named MOSFIT using GALENE-III[2] as the main device simulator. In the input processor of GALENE-III there is a structure file which contains device structure information including doping profiles, gate oxide thickness and so on. A two-dimensional doping profile is expressed by combination of simple functions like step, Gaussian and error functions without using any complicated 2-D spline functions suggested by others[1]. 1-D channel doping $N_{ch}(x)$ is defined as

$$N_c(x) = N_c \begin{cases} \exp\{-(\frac{x-x_c}{D_{c1}})^{E_{c1}}\} & (x \le x_c) \\ \exp\{-(\frac{x-x_c}{D_{c2}})^{E_{c2}}\} & (x_c \le x) \end{cases} \quad (1)$$

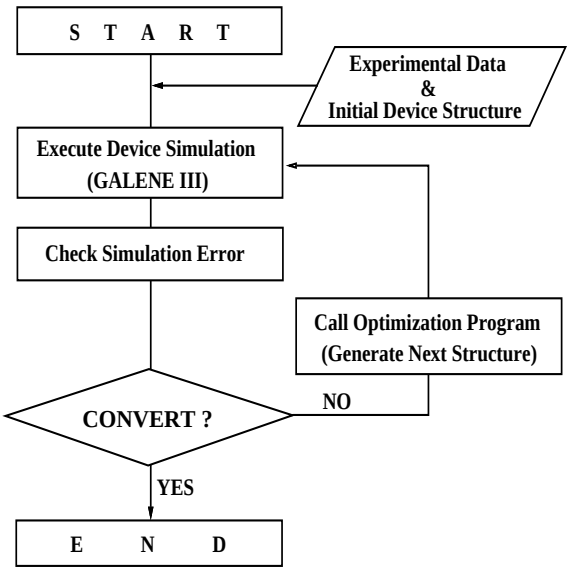

Fig. 1. Program Flow of MOSFIT

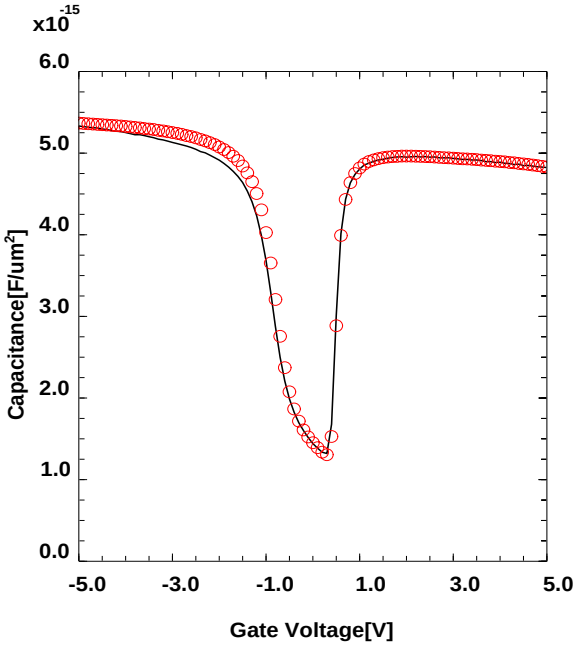

Fig. 2. C-V simulation after the gate oxide thickness and the poly-gate doping profile are determined (solid lines : mesurement, symbols : simulation).

$$N_s(x) = N_s \exp\{-(\frac{x - x_s}{D_s})^{E_s}\} \tag{2}$$

$$N_{ch}(x) = N_c(x) + N_s(x) \tag{3}$$

where N_c, N_s, x_c, D_{c1}, D_{c2}, D_s, E_{c1}, E_{c2}, E_s are fitting parameters and x_s is a coordinate of silicon surface. Poly-Si gate doping $N_p(x)$ is defined as

$$N_p(x) = N_g \begin{cases} 1.0 & (x \le x_g) \\ \exp\{-(\frac{x-x_g}{D_g})^{E_g}\} & (x_g \le x \le x_{gs}) \end{cases} \tag{4}$$

where x_{gs} is a coordinate of gate-SiO2 interface and N_g, x_g, D_g, E_g are fitting parameters. And 2-D source/drain extension $N_{ex}(x, y)$ doping is defined as

$$N_1(x, y) = \frac{N_1}{2} \exp\{-(\frac{x - x_1}{D_1})^{E_1}\} \operatorname{erf}(-\frac{y \mp y_1}{R_1}) \tag{5}$$

$$N_2(x, y) = \frac{N_2}{2} \exp\{-(\frac{x - x_2}{D_2})^{E_2}\} \operatorname{erf}(-\frac{y \mp y_2}{R_2}) \tag{6}$$

$$N_{ex}(x, y) = N_1(x, y) + N_2(x, y) \tag{7}$$

where $\operatorname{erf}(-\frac{y-y_0}{R})$ is error function and N_1, N_2, x_1, x_2, D_1, D_2, E_1, E_2, y_1, y_2, R_1, R_2 are fitting parameters.

The inverse modeling procedure by MOSFIT shown in Fig.1 is described as follows. At first a MOSFET device structure and its doping profiles in the structure file are expressed by those functions using a process simulator output as an initial guess. C-V or I-V characteristics are calculated and compared with experimental results. Then the MOSFIT calculates the error and corrects the fitting parameters in those functions in the structure file by the optimization program to generate a new device structure. Then again C-V or I-V characteristics are calculated and compared with the experimental results. These steps are iterated until enough convergence is obtained. Finally when it is converged, the structure file contains an inversely extracted device structure concerning the calculated electrical characteristics.

III. How to Extract a Sub-Quarter Micron Device Structure

In order to obtain a complete device structure for a deep sub-micron range, the procedure described in the previous section is applied to at least three different device structures. The first one is a large area MOSFET to extract a gate oxide thickness and a poly-gate doping profile by using split C-V measurement data. The second one is a long channel MOSFET to extract a channel doping profile by using a body effect of sub-threshold Id-Vg characteristics. And, the third one is a wide channel or finger gate MOSFET to extract a source/drain profile as well as a poly-gate length by using split Cgd-V (channel capacitance) characteristics.

Figure 2 shows an example of C-V characteristics for a large area MOSFET(capacitance). The gate oxide thickness is determined to fit the capacitance value at the maximum voltage in the accumulation region. Then we can obtain good agreement in the inversion region optimizing the poly-gate doping profile without considering a quan-

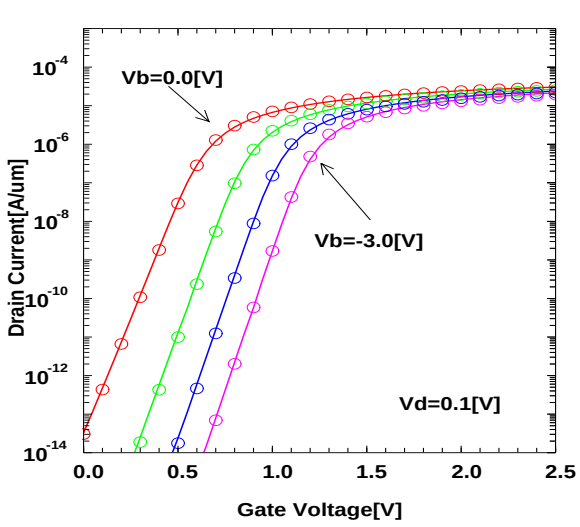

Fig. 3. Channel profile fitting by a body effect in the sub-threshold regime (solid lines : mesurement, symbols : simulation).

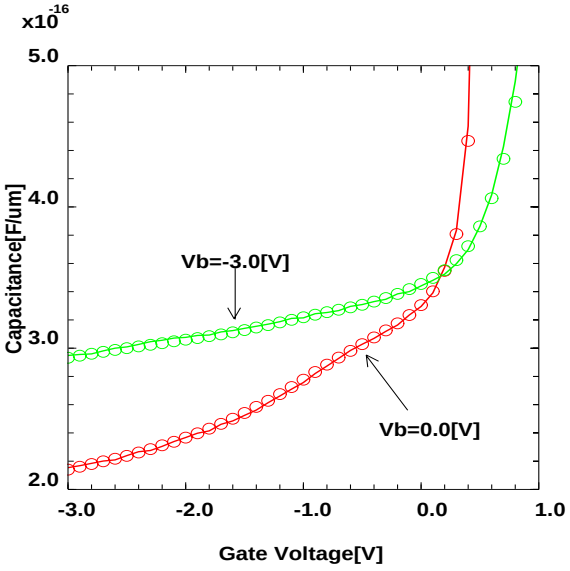

Fig. 4. Source drain extension doping profile fitting using Cgd-V characteristics (solid lines : mesurement, symbols : simulation).

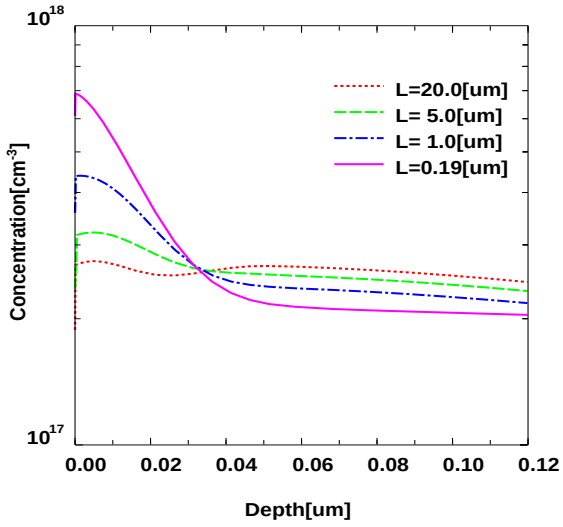

Fig. 5. Channel length dependent doping profiles

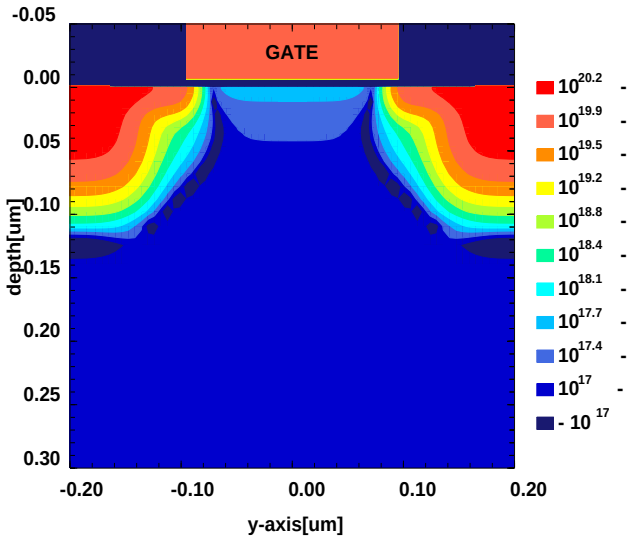

Fig. 6. Extracted result of the 2D-doping profile of a 0.19μm nMOSFET

tum mechanical effect which is effectively included in the gate doping and oxide thickness value.

Figure 3 is an example of channel profile fitting using the body effect of a 1.0μm(Lg) MOSFET. This good fitting guarantees the accuracy of the channel profile for a reasonable range in depth. In Fig.4 source/drain extension doping profile fitting is demonstrated by Cgd-V characteristics of a finger gate MOSFET for different substrate bias conditions.

In the case of deep submicron devices it is well known that transient enhanced diffusion(TED) causes channel impurity redistribution and boron pile-up occurs just in the vicinity of source/drain junction. The TED is thought to be the main reason for a reverse short channel effect. In order to express it, the channel profiles should be different from that of a long channel transistor. By changing the channel profile to fit the body effect for each shorter channel device, we can obtain the channel length dependent doping profiles as shown in Fig.5. In our approach channel doping profile is represented by 1-D functions, so we consider that obtained functions express doping profiles averaged along the channels.

Figure 6 shows the final two-dimensional doping profile and the device structure for a 0.19μm(Lg) MOSFET.

In order to express linear Id-Vg characteristics for a deep sub-micron device we must consider a parasitic resistance effect which cannot be included in the final device structure. In the case of a salicide device structure silicide layers are formed on the source/drain contact regions. We include a silicide-to-silicon contact resistance which is treated as a low mobility region defined as shown in Fig.7. The mobility value is determined to reproduce

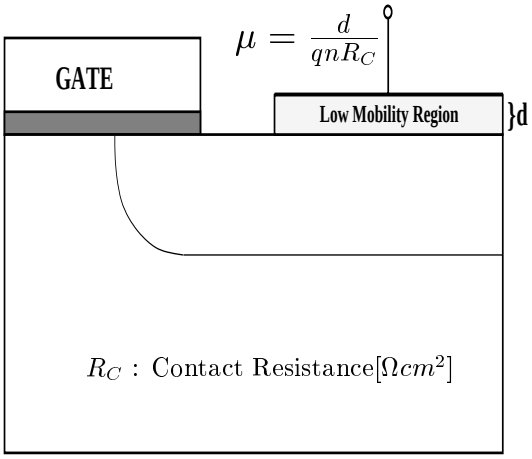

Fig. 7. Treatment of the contact resistance in the device simulation

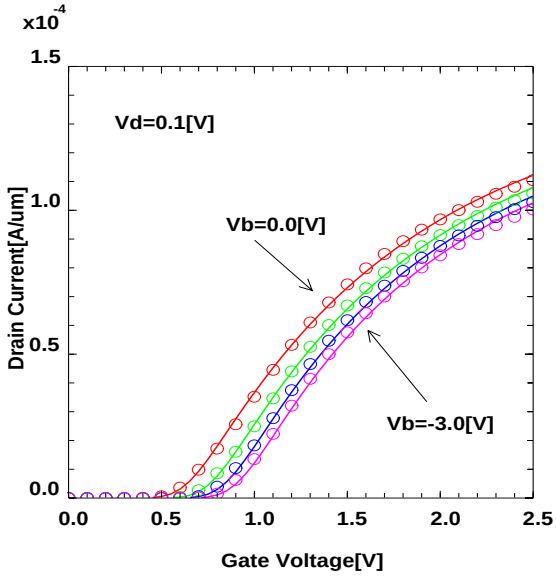

Fig. 8. Id-Vg simulation in the linear regime for contact resistance extraction (solid lines : mesurement, symbols : simulation)

the Id-Vg characteristics in the linear regime including the body effect (Fig.8)

Final results are guaranteed by looking at the saturation Id-Vd characteristics in Fig.9 and substrate current characteristics in Fig.10. The Id-Vd simulation is performed by GALENE-III and the substrate currents are calculated by the full-band Monte Carlo device simulator FALCON using the inversely modeled device structure[3]. Because of the uncertainty of the high field mobility in the generalized hydrodynamic model implemented in GALENE-III[4] there is a slight discrepancy of the saturation drain current between the measurement and simulation. However, this discrepancy is not serious.

We can show that our approach is not only able to reproduce the experimental results but also able to predict I-V characteristics of differently processed devices. Figs. 11 and 12 show the example comparing the predicted and experimental I-V characteristics for saturation drain current and substrate current when the implant dose of the source/drain extension is decreased to one-tenth. The predicted device structure in which peak values N_1, N_2 in Gaussian functions (5,6) are decresed to one-tenth reproduces the terminal current voltage curves so well that we can investigate what kind of device process should be chosen to satisfy required device specification using one well performed inverse modeling result.

IV. Conclusion

We have shown a simple inverse modeling approach using Gaussian/error functions to express two-dimensional doping profiles without complicated 2-D spline functions suggested by others. We also included poly-gate doping to express effective gate oxide thickness without using quantum mechanical calculation to solve self-consistent Poisson and Schrödinger equations. Not only drain current but also substrate current results have guaranteed the accuracy of finally extracted sub-quarter micron device structures including their doping profiles. Our approach can also predict device performance to optimize its structure for required specification.

References

[1] N. Khalil et al., "Inverse Modeling Profile Determination: Implementation Issues and Recent Results", *International Conference on Simulation of Semiconductor Processes and Devices(SISPAD)*, pp.19-22(1996)

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[3] Chr. Jungemann et al., "Accurate Prediction of Hot-Carrier Effects for a Deep Sub-μm CMOS Technology Based on Inverse Modeling and Full Band Monte Carlo Device Simulation", *International Conference on Simulation of Semiconductor Processes and Devices(SISPAD)*, pp.59-60(1996).

[4] GALENE-III User's Guide Version 2.5

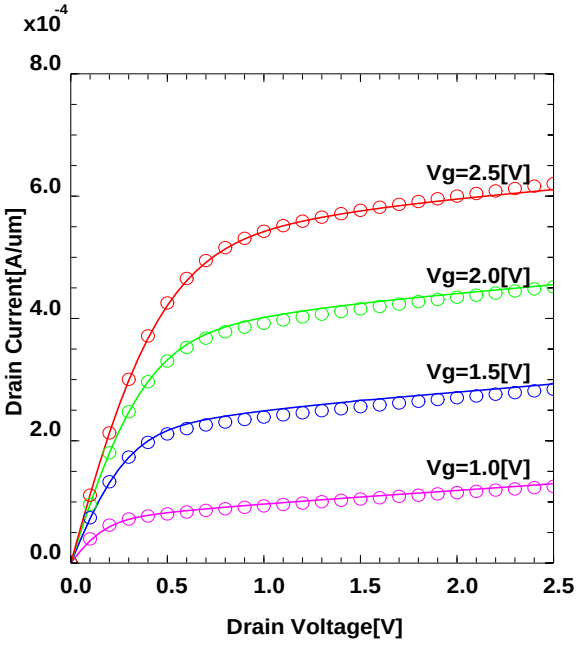

Fig. 9. Id-Vd simulation for the extracted 0.19μm nMOSFET structure (solid lines : mesurement, symbols : simulation)

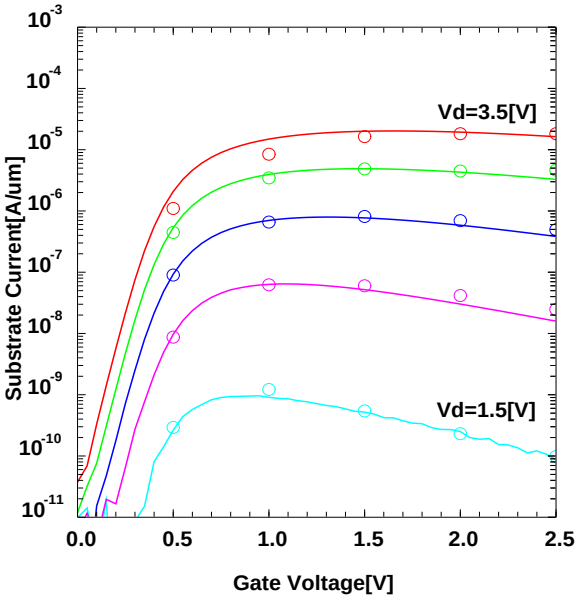

Fig. 10. Substrate current simulation for the 0.19μm nMOSFET structure by the full-band MC simulator FALCON (solid lines : mesurement, symbols : simulation)

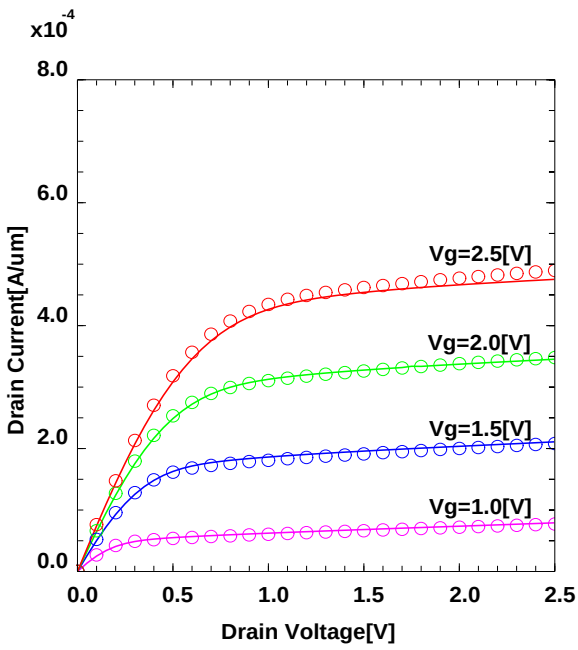

Fig. 11. Id-Vd simulation for the device with the scaled S/D extension profile by a factor of 0.1 (solid lines : mesurement, symbols : simulation)

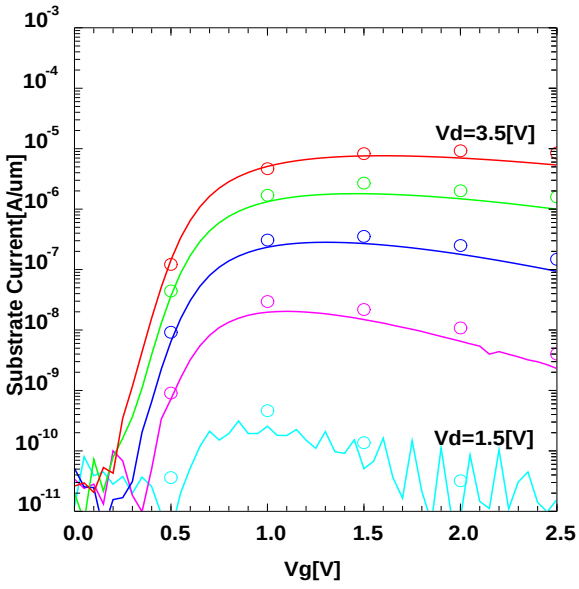

Fig. 12. Substrate current simulation for the device with the scaled S/D extension profile by a factor of 0.1 (solid lines : mesurement,symbols : simulation)