# A CSIC Implementation with POCSAG Decoder and Microcontroller for Paging Applications

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**Abstract — This paper presents a CSIC (Customer Specification Integrated Circuit) implementation, which includes a 512/1200/2400 bps POCSAG decoder, PDI2400 and MC68HC-05 changed by PANTECH.**

**It can receive all the data with the rate of 512/1200/2400 bps of a single clock of 76.8 KHz. It is designed to have maximum 2 own frames for service enhancement. To improve receiver quality, a preamble detection considering frequency tolerance and a SCW (Synchronization Code Word) detection at every 4 bit is suggested. Also we consider an error correction of address and message up to 2 bits. Furthermore, it is possible with proposed PF (Preamble Frequency) error to achieve a battery life increase due to the turn-off of RF circuits when the preamble signal is detected with noises. The chip is designed using VHDL code from PDI2400 micro-architecture level. It is verified with VHDL simulation software of PowerView™. Its logic diagrams are synthesized with VHDL synthesis software of PowerView™.**

**Proposed decoder and MC68HC05 CPU of MOTOROLA are integrated with about 88000 transistors by using 1.0um HCMOS process and named MC68HC05PD6. It is proved that the wrong detection numbers of preamble of noises are significantly reduced in the pager system that uses our chip through the real field test. The system receiving performance is improved by 20% of average, compared with other existing systems.**

## I. INTRODUCTION

There are two kinds of portable communication systems. That is, one is possible to send and receive signals and the other is only possible to receive them. Pager belongs to the later and is still a growing market very rapidly in the whole world because of its convenience and low cost[1]. The number of subscribers up to 1994 is 6.5 million and will be increased by 10 million in 1995 for the Korea market.

Figure 1 shows a pager block diagram with three major blocks. The first one is RF input circuits that can transform RF signal from the base station into digital signal. The POCSAG (Post Office Code Standardization Advisory Group)[2] decoder analyzes this digital signal and compares it with own address. The last one is MCU (Micro Controller Unit) circuits that notify subscriber of the information and control the system.

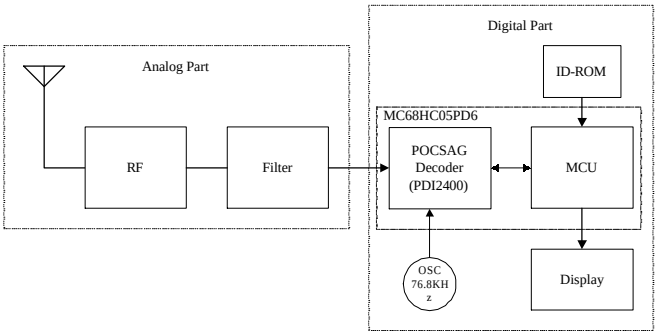


Fig. 1. Block diagram of pager

In this paper, a new POCSAG decoder is suggested that can minimize both its size and power dissipation with improved receiver sensitivity. Currently, most of commercial decoders provide the data rate of 512/1200 bps. On contrast, 2400 bps rate system is highly required to meet the increasing number of subscribers. However, a clock generator that is 2 times faster than existing decoder of 512/1200 bps rate should be employed to increase the rate by 2400 bps. Since most of decoders have only one own frame, additional own address is necessary for giving supplementary public service such as weather forecast and stock information. In addition, while the error correction of the address is performed up to 2 bits, the error correction of message is done up to 1 bit. That is one of the reason to cause the receiver sensitivity to be reduced.

The suggested decoder is designed with single clock of 76.8KHz to receive all the data transmitted with 512/1200/2400 bps. Moreover, the design of the decoder allowed two own frames to be assigned in order that various public services are available. On the other hand, to improve receiver quality, a preamble detection considering frequency tolerance and a SCW (Synchronization Code Word) detection at every 4-bit is suggested. Also we consider an error correction of address and message up to 2 bits. Furthermore, it is possible with proposed PF (Preamble Frequency) error to achieve a battery life increase due to the turn-off of RF circuits when the preamble signal is detected with noises.

In this paper, the design procedures are shown in figure 2. In order to verify the precise operation and receiving

quality of decoder, it is implemented with 1 FPGA using FLEX81188GC232-3 of ALTERA company[8]. The FPGA decoder employs to implement a pager. The usefulness of this paper is proved through the shield room test and field test of the pager. The decoder is implemented with a single chip that use 1.0um double poly/single metal process, combining the commercially available MC68HC05 CPU core.

This paper is organized as follows. In section II, POCSAG signal rules and operation modes are described, followed by the suggestion of the decoder configurations and functions. Then its hardware implementation and performance evaluation are discussed. Finally, MCU and POCSAG decoder are implemented with CSIC (Customer Specification Integrated Circuit).

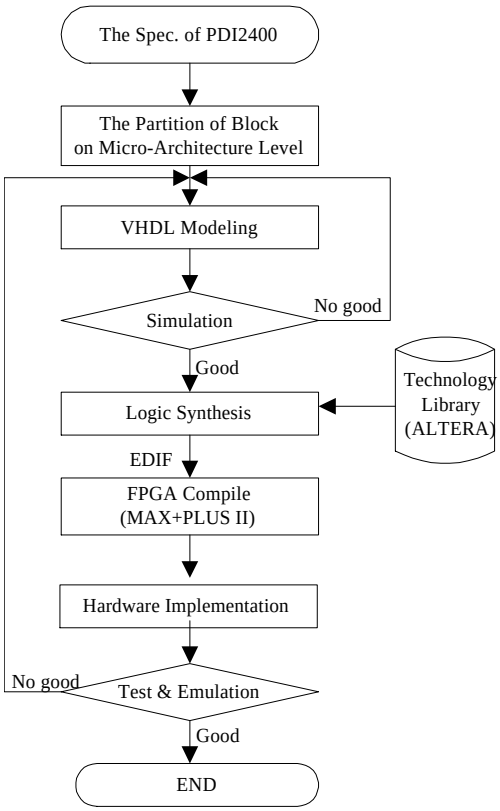


Fig. 2. Design flow of the POCSAG decoder

## II. POCSAG CODE FORMAT[2]

The POCSAG signaling system is the most popular for paging signal and the standard is defined by CCIR recommendation 584-1. The structure is illustrated in figure 3. The POCSAG signal consists of a preamble followed by one or more batches. A batch is composed of SCW of 32 bits and 8 frames. Each frame is composed of 2 code words. One code word is composed of 32 bits.

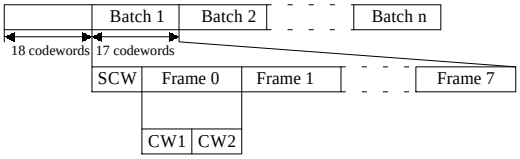


Fig. 3. POCSAG signal format[1]

The data receiving of pager begins with receiving of preamble signals more than 576 bits that are composed of "1010 ..." such as replica of "10" from a base station. Once preamble signal is detected, it waits for receiving SCW that is used to synchronize 8 frames for timing control. After receiving SCW, it compares a received data from own frame with own address information. Then if they are matched, it interprets the received data in consecutive frames as message information. The code words of batch are divided into 3 types. The first one is SCW of hexa-decimal 7CD215D8 that is defined to synchronize beginning. The second one is ICW (Idle Code Word) of hexa-decimal 7A89C197 that is defined to designate the end of receiving process. Finally, the third one is a code words that present address or message data and is shown in figure 4.

| Bit No. | 31 | 30 - 13 | 12 - 11 | 10 - 1 | 0 |
|---|---|---|---|---|---|
| Address codeword | Address Flag = 0 | Address Bits | Function Bits | BCH Check Bits | Even parity |
| Message codeword | Message Flag = 1 | Message Bits | | BCH Check Bits | Even parity |

Fig. 4. Code word format[1]

Address and message data are defined to perform the error correction with BCH (31,21) algorithm. The high level 21 bits of each code words is address or message data and the remaining 10 bits is redundancy for BCH error correction. Considering this receiving process, we define the operation of the PDI2400 as 4 modes.

## III. ARCHITECTURE AND FUNCTION OF PDI2400

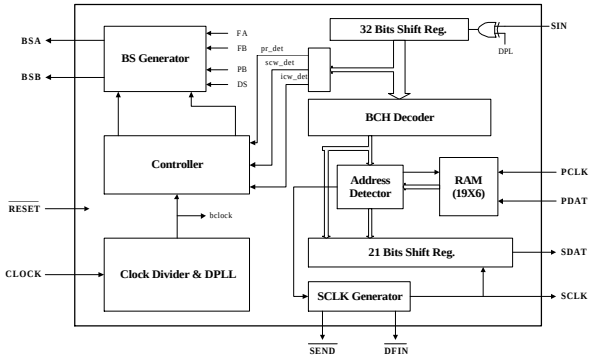


Fig. 5. The architecture of the PDI2400

The internal architecture of PDI2400 is defined as in figure 5 considering the conception of operation modes, BCH error correction, interface with MCU, and the generation of control signals for low power. The functions and hardware designs of each block in figure 5 are as follows.

### *A. Detection of Preamble Signal and SCW*

Synchronization timing for batch data is determined based upon advance received preamble signals. Further, the synchronization timing of beginning of the frame is determined by the detection of SCW.

Detecting with consecutive bits input of "101010...", the PDI2400 considers as establishing preamble signal. To improve the receiving quality, we took account into duty factor of preamble pattern and frequency tolerance of preamble on design. The value of tolerance of frequency is determined through a number of test. If frequency tolerance of preamble is large, the ratio of preamble detection is improved and the ratio of noise detection is high. Then, we chose frequency tolerance of 9%. Figure 6 presents the signal detection method considering the above 2 factors. Third, although the preamble signal is detected under WAIT or RECEIVE mode, if the PF error occurs in the preamble data patterns that detected in PREAMBLE mode, it transits to WAIT mode regardless of the received preamble signal. The PF error is defined as the occurrence of 3 consecutive errors of 1 error that is defined as the case that data with 2 or more times more frequency than preamble frequency during "10" pattern time are received. Figure 7 shows an example of PF error.

In order to detect SCW, the inputted 32 bits data is divided into 4 bits unit. Then, comparing the bits with the SCW defined with 7CD215D8, the numbers of errors are counted within 4 bits unit. It is defined that the SCW is detected if there are within 3 errors. Note that ICW detection methods are designed with the same methods as SCW detection methods.

### *B. BCH (31,21) Decoder[3-5]*

The message codeword and the address codeword are defined in figure 4. Therefore it is necessary to design a decoder with BCH (31,21) algorithm as in figure 8.

The first step to decode is calculate the syndrome s(x) defined as

$$s(x) = (s_1, s_2 \ldots s_{2t}) = r(x) * H^T \quad (1)$$

, Where r(x) is including errors through a channel and can be expressed as (2).

$$r(x) = c(x) + e(x) \quad (2)$$

The syndrome is defined as (3).

$$r(x) = q(x) * m(x) + s(x) \quad (3)$$

In (3), m(x) is $m_1(X)=1+X^2+X^5$, $m_3(X)=1+X^2+X^3+X^4+X^5$. The q(x) is quotient and s(x) is remainder. Error correcting capability, t of BCH(31,21,2) is equal to 2, so number of syndrome becomes 4. That is $S(x)=(s_1,s_2,s_3,s_4)$.

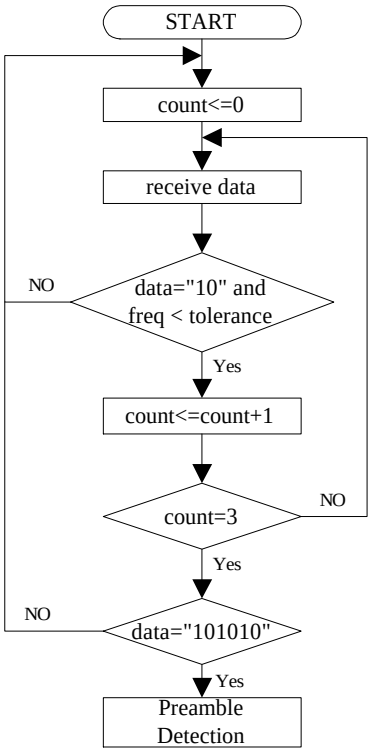


Fig. 6. The preamble detection method

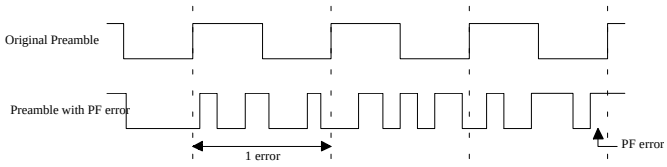


Fig. 7. Detection of PF error

Just two elements of s1 and s3, which are remainders of divided by $m_1(x)$ and $m_3(x)$ respectively are used. Error location equation after obtaining the syndrome is calculated as in expression (4).

$$\sigma(x) = \sigma_0(x) + \sigma_1(x) + \ldots + \sigma_t(x) \quad (4)$$

The root of $\sigma(x)$ can be acquired using expression (5), and Chiens circuit was used for hardware implementation.

$$\sigma(x) = 1 + s_1 x + (s_1^2 + (\frac{s_3}{s_1}))x^2 \quad (5)$$

Since σ(x)=1 for $s_1=s_3=0$, there are no errors. However, it means there is one error if $s_1\neq0, s_3=s_1^3$. Further, it means there are errors more than 2 if $s_1\neq0, s_3\neq s_1^3$. Note that the root of error polynomial equation designates the error location.

In PDI2400, BCH encoder is embedded for two error corrections. Here the decoded 21 information bits are encoded and theregenerated parity bits are compared with received data include less than two errors. Error corrected

21 bits are divided by polynomial $1+x^3+x^5+x^6+x^8+x^9+x^{10}$ and the remainder is compared with 10 bit-long parity. If two patterns are same, it means that less than 2 bits errors is corrected successfully.

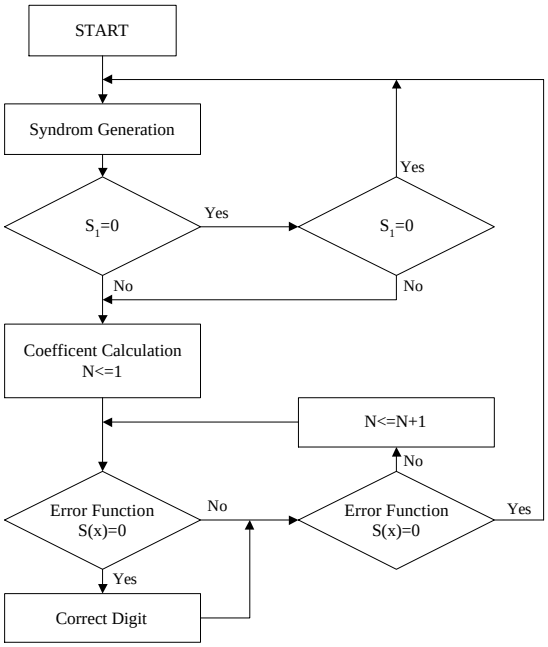


Fig. 8. Flowchart of BCH decoding

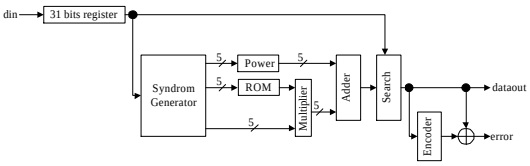


Fig 9. Block diagram of BCH decoder

### *C. Generation of Battery Saving Signal*

To reduce power dissipation of the pager, a control signal that turns on or turns off RF circuits is generated from POCSAG decoder. PDI2400 generates the BSA and the BSB as battery saving signals. BSA is used for general purposes, but BSB is a signal for PLL-type wide area pager for the future usage. There is no difference except that the signal width of BSB is larger than that of BSA. The generation of BSA depends on the operation modes. The "0" signal is generated for PROGRAM mode. That is, since RF circuits do not need to receive the data, it might be turn-off. On contrast, since the RF circuits on WAIT mode should be turn-on every batch time in order to detect the preamble signal existence, such a signal as shown in figure 10 is generated.

A generated signal on PREAMBLE mode is always "1" because the SCW must be detected. On RECEIVE mode, only data receiving happens during the own frame. Thus, the signal is held as "1" during own frame. Advance time starting as "1" is differently defined based on each bps. That is, it was defined in PDI2400 as "to have maximum 2 own frame for 1 batch." In this case, assuming the own frames are assigned as 1 and 5, the generation of BSA on RECEIVE mode becomes as in figure 11.

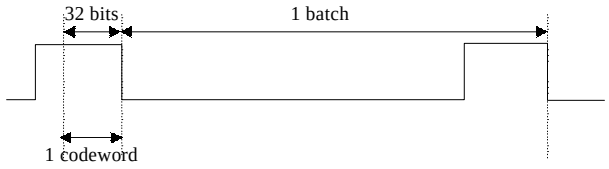


Fig. 11. BSA timing on WAIT mode

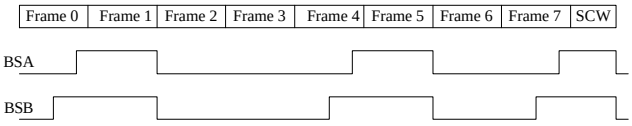


Fig. 12. Battery saving timing when self-frames are 1 and 5.

### *D. Generation of Internal Clock*

In PDI2400, the internal clock is generated to meet the required operation speeds from external clock of 76.8KHz. It can be implemented with counter circuits. According to X value that can be yielded form (6), internal Bclock of one hundred fifty clocks with a period of 76.8KHz for 512bps is generated.

$$X = \frac{76.8KHz}{data\ rate} \tag{6}$$

Furthermore, Bclock is designed to have sixty-four clocks for 1200bps and thirty-two clocks for 2400bps, respectively.

### *E. Internal Controller Module*

The design of FSM (Finite State Machine) requires to provide 4 operation mode transitions. Further, the FSM should meet the transition between each states involving 17 code words of 1 batch to be a state.

## IV. Hardware Implementation and Performance Evaluation

### *A. FPGA Emulation*

Micro-architecture circuits of each block defined in chapter 3 were configured. Then they are described with

VHDL[6]. Their verification is performed with simulation software[7] of PowerView™. To verify PDI2400 hardware systems, FPGA is implemented. The logic circuits for verified VHDL code are generated by using PowerView™ logic synthesis software[7]. Single ALTERA[8] FLEX81188-GC232-3 is employed for FPGA. The placement and the routing with MAX+PLUS II result in the usage rate of 98%.

Integrating the PDI2400 and the PP-X03 RF circuits, a pager is implemented in PANTECH company. For performance evaluation, shield room test is carried out and compared with other PP-X03 with NPC decoder[9]. Shield room test results in the similar sensitivity as shown in figure 13, but its numbers of recognition as preamble for noises are significantly reduced as in table 1. Thus, it is expected to increase the battery life time. Moreover, the field testing was performed with PDI2400's, domestic products and foreign products. According to the result of testing, PDI2400's one received 77 calls of the total 84 calls. The receiving ratio of PDI2400's one was 91.7%. In case of domestic products, those received 280 calls of 420 calls. That of those was 66.7%. Foreign products received 128 calls of 164 calls. That of those was 76.2%. As the results, PDI2400's one showed more 20% receiving ratio than that of other companies.

TABLE 1
The number of preamble detection with noises for 200sec.

| | 512bps | 1200bps | 2400bps |
|---|---|---|---|
| PP-X03 | 12 | 35 | Not supported |
| PDI2400 | 4 | 24 | 74 |

Considering such performance evaluation, the usefulness of the PDI2400 POCSAG decoder that is implemented with the method of this paper is proved.

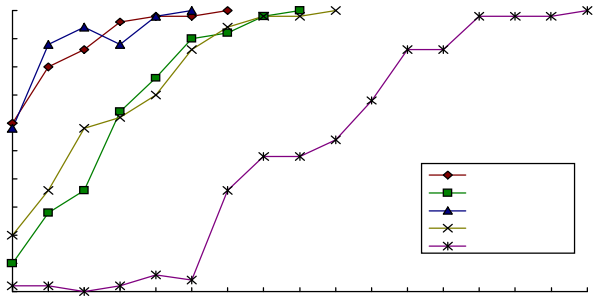

Fig. 12. The results of sensitivity test in shield room

### *B. CSIC Implementation*

The designed decoder of PDI2400 was implemented with FPGA, and performance evaluations were performed.

In addition, to realize more less size and more less power dissipation than the commercially used pagers, single chip CSIC was implemented. For the CPU core of CSIC, MC68HC05 CPU of MOTOROLA is used. The chip integrated LCD driver, 512 bytes RAM, 16K bytes ROM, eight 8 bits ports and 8/16 bits timer, watch dog timer, and serial communication interface.

It is fabricated by using MOTOROLA process technology that is supporting 1.0um HCMOS double poly and single metal. Its die size is 292mil x 342mil that includes 88,000 transistors. The PDI2400 size is 158mil x 48mil with about 14,000 transistors. The employed package type is TQFP with 80 pins of 12mm x 12mm. It is named as MC68HC05PD6. Figure 13 shows the layout diagram of MC68HC05PD6.

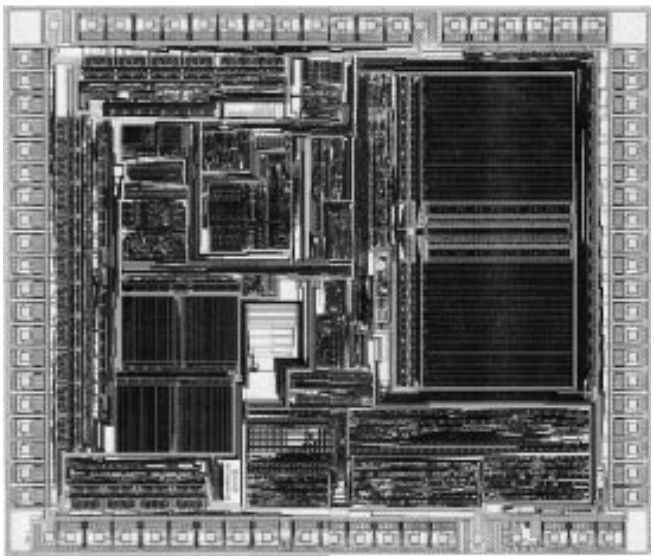

Fig. 13. The layout design of MC68HC05PD6

## V. CONCLUSION

In this paper, It was shown that POCSAG decoder, PDI-2400, which were fabricated on a single CSIC chip with MOTOROLA 68HC05 CPU core was designed and its performance evaluation was performed.

PDI2400 receives all the data transmitted with the rate of 512/1200/2400 bps using single clock of 76.8KHz. The system including two own frames was designed to be provided with various public services such as weather forecast or stock information. Furthermore, in order to improve receiver sensitivity, the error correction up to 2 bits for both address and message information was done. Preamble signal was detected considering frequency tolerance and SCW was detected every 4 bits. Furthermore, it was possible with proposed PF (Preamble Frequency) error to achieve a battery life increase due to the turn-off of RF circuits when the preamble signal is detected with noises.

VHDL modeling was performed for hardware design with VHDL softwares of PowerView™.

To evaluate the precise operation and performance of the suggested decoder, it was implemented with FPGA

using one FLEX81188GC232-3. The pager with implemented decoder was tested both in the shield room and in the field. It was shown from the test results that its performance was about 20% better than the commercially available pagers.

The suggested decoder was fabricated in a single chip with integration of MOTOROLA MC68HC05 CPU core. The employed process technology for the fabrication is Motorola HCMOS double poly/single metal process technology. The chip integrated about 88,000 transistor and is named as MC68HC05PD6.

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