Routing for Manufacturability

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Abstract

The impact of spot defects on the susceptibility for electrical failure of a net is analyzed. Based on this analysis, a general routing cost function is presented, in which the manufacturability of a net is taken into account in conjunction with the traditional routing objectives. The new cost function, relating the process spot defects to the routing procedure has been implemented. For the benchmark layouts obtained by both the original routing tool and the new routing module, the failure probabilities are analyzed. The results show that the failure probability of a layout is significantly decreased if the spot defect mechanism is taken into account in the routing procedure, while the area of the layout is kept constant.

1 Introduction

Routing a net is a "classical" topics in CAD for VLSI. The problem can be formalized as the *Minimum Steiner Tree* problem in an appropriate routing graph [Len90]:

Problem: Minimum Steiner Tree
Instance: A connected undirected graph $G(V, E)$, also called routing graph, with edge cost function $\lambda : E \rightarrow \mathbb{R}_+$ and a net $N \subseteq V$, consisting of vertices to be connected.
Configurations: All edge–weighted trees.
Solutions: All Steiner trees for N in G, denoted as E_T, i.e. all trees of G connecting all vertices of N with all its leaves being vertices in N.
Minimize: $\lambda(T) = \sum_{e \in E_T} \lambda(e)$

Many algorithms exist to solve the minimum Steiner tree problem, see [Hwa92] for an excellent overview. All of these algorithms will come up with significantly different routings if different cost functions are applied. Conventionally, the edge cost function $\lambda(e)$ is defined as the product of the distance d between two adjacent vertices and a control factor c, i.e. $\lambda(e) = cd$. Parameter c is used to adjust the edge weights in or between the different mask layers. For example, by setting a larger value of c for the poly layer and a smaller value of c for the metal layer, connections with high signal propagation speed can be obtained instead of a real shortest path in distance. Furthermore, by choosing different values for c for different routing directions, thus favoring certain directions, a routing style can be imposed. Summarizing, the traditional cost function can affect a routing in three aspects, viz. (1) the net length, (2) the performance and (3) the routing style.

As process feature size keeps decreasing and IC chips are becoming more complex, chips are more sensitive to process disturbance. *Inductive Fault Analysis* [She85] reveals that close nets are likely to get shorted because of spot defects, the main local disturbance in fabrication processes. Therefore, from the point of view of defect analysis, the yield of a good routing depends not only on the net itself, but also on the environment of the net. In other words, the minimization of the cost of a net in terms of the net length is not the optimal solution if the failure possibility of the net is taken into account. Obviously, the proposed cost function $\lambda(e)$ does not adequately cover this issue.

The idea to relate the routing procedure to the process defects was first proposed in [Pit89]. A channel router called DTR (Defect Tolerant Routing) was implemented to minimize the critical areas between the horizontal routing segments. Later on, the authors [Bal91] tried to minimize the critical areas between both the horizontal segments and the vertical segments by searching for *valid gaps* in routing channels. In both papers, there are still quite a few drawbacks that make the routing results far from being effectively defect–tolerant. The main reasons are:

1 Only spot defects causing extra materials (bridges) are considered. Consequently, when the probability of the bridge faults decreases by minimizing the critical area for the bridges, the probability of the open faults, caused by missing materials, probably increases.
2 Only the single layer defect model is used for modeling the spot defects. The fact that in addition missing material or extra material between mask layers will give rise to more bridges or opens is not taken into account.
3 The trade–off between the increase of the number of vias (potential open sites) and the decrease of the critical areas for bridges is not considered.
4 Only one defect size is considered. However, the spot defects are distributed with random sizes in reality. To accurately model spot defects, it is important to take into account the defect size distribution.

In this paper, according to the defect size distribution and the process statistics, the failure probability of a net is analyzed. Based on the analysis, we propose a new edge cost function for the general routing problem. By applying the new cost function, a good trade–off between the minimization of the net length and the minimization of the failure probability can be obtained for each net, which consequently leads to a better layout manufacturability.

2 Spot Defects

The functional failure of a chip is likely caused by spot defects [Str89]. The result of a spot contamination in a process step is either extra material or missing material at the place where the spot occurs [Mal85]. A spot defect may either occur in one layer of the silicon structure, such as the metal layer or the poly layer, or somewhere between two layers, where it causes extra or missing oxide. We classify spot defects as follows:

1 *One layer extra material defects (OE)*: The defects may cause the bridges between connection patterns in the same layer. For example, the spot defect with size d in the metal layer will result in a bridge between nets 1 and 2 as shown in Figure 1(a).
2 *One layer missing material defects (OM)*: The defects will result in open faults if the spot defects break the connection patterns in one layer. Such a case where a spot defect breaks a net in the metal layer is shown in Figure 1(b). If the defects cause missing via patterns, the open faults will also be induced because of missing vias.
3 *Inter–Layer extra oxide defects (IE)*: If the defects occur in the oxide at the location of vias, the vias may be blocked, thus leading to open faults. Figure 2(a) shows an example where a via connecting metal 1 and metal 2 is broken by the spot defect.

4 *Inter–Layer missing oxide defects (IM)*: The defects are also referred to as *oxide pinholes*. If the defects occur in the oxide between two overlapping conductors, the conductors are shorted. For instance, the pinhole in Figure 2(b) causes a new via connecting metal 1 and metal 2, and therefore results in a bridge.

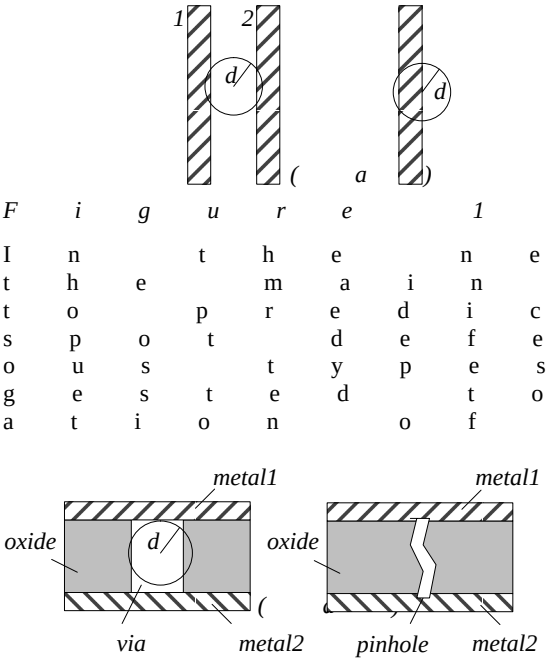

Figure 2 (a) Fault type IE. (b) Fault type IM.

3 The Failure Probability of a Net

Critical area, defined as the area in which the center of a defect must fall to cause a fault, can be extended to the critical area with respect to a particular *object*. The object can be any spot defect type. Suppose the spot defect size distribution for object η is $D_\eta(x)$, and the critical area with respect to object η is $A_\eta(x)$, where x is the spot defect size. If a uniform defect density P_η is assumed, then the probability of the failure of object η, denoted as F_η, can be expressed as:

$$F_\eta = P_\eta \int_{min}^{max} D_\eta(x) A_\eta(x) dx$$

where *min* and *max* are the minimum and the maximum defect sizes. There have been many efforts on modeling the defect size distribution. In this paper, the size distribution function taken from [Sta84] is assumed. In principle, using other size distribution functions will not affect the following discussions. By replacing function $D_\eta(x)$ with X_0^2/x^3, where X_0 is a process–related parameter, we obtain

$$F_\eta = P_\eta X_0^2 \int_{min}^{max} A_\eta(x) \frac{1}{x^3} dx \qquad (1)$$

As described in the previous section, the spot defects can be classified by four types. For each net, the critical area $A_\eta(x)$ with respect to the spot defects of type η can be estimated by using the virtual artwork concept proposed in [Mal85]. Hence, the failure probability for each type of spot defect can be computed according to equation (1).

Given a net N, suppose the net length is l, and the net width and spacing are w and s respectively. Assume b is the total length of the adjacent segments with the neighboring nets, and o is the number of overlapping sites, i.e. the number of unit area overlaps with the conductors in the upper or lower layer as shown in Figure 3. In addition, we suppose the number of vias on net N is v.

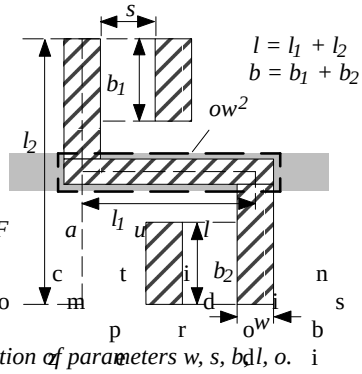

Figure 3 Explanation of parameters w, s, b, l, o.

1 Type OE: If the defect size x is smaller than s, then the defects will not cause any fault due to the zero critical area. If $s \le x < 2s + w$, the critical area $A_{OE}(x)$ is equal to $(x - s)b$. However, when the defect size is equal or larger than $2s + w$, the critical area will be saturated to $(s + w)b$. Consequently, the probability of the failure of defect type OE is

$$F_{OE} = P_{OE} X_0^2 b \left(\int_s^{2s+w} \frac{x-s}{x^3} dx + \int_{2s+w}^{max} \frac{s+w}{x^3} dx \right)$$

By setting *max* to ∞, we obtain $F_{OE} = \alpha b$, with

$$\alpha = \frac{P_{OE} X_0^2}{2} \left(\frac{1}{s} - \frac{1}{(2s + w)} \right) \qquad (2)$$

2 Type OM: When the defect size is smaller than w, it is not possible that the net will be broken by the defect. Therefore the critical area is zero. For the defects with size x, $w \le x < 2w + s$, the critical area $A_{OM}(x)$ is equal to $(x - w)l$. As the defect size exceeds $2w + s$, the critical area will be saturated to $(w + s)l$, similar to the defect type OE. Consequently the probability of the failure caused by the defects of type OM can be described as

$$F_{OM} = P_{OM} X_0^2 l \left(\int_w^{2w+s} \frac{x-w}{x^3} dx + \int_{2w+s}^{\infty} \frac{s+w}{x^3} dx \right)$$

Similarly, we derive $F_{OM} = \beta l$, where

$$\beta = \frac{P_{OM} X_0^2}{2} \left(\frac{1}{w} - \frac{1}{(2w + s)} \right) \qquad (3)$$

3 Type IE: Since the defects of type IE will only break conductors traversing the oxide, i.e. vias, the probability of the failure caused by this type of defects is proportional to the number of vias on the net. It needs mentioning that the defects in oxide follow no longer the normal size distribution function. Here, we assume a simple model to estimate the failure probability[1]. Suppose the size of a via is $w \times w$. The probability of failure can be estimated by $F_{IE} = \gamma v$, where

$$\gamma = P_{IE} w^2 \qquad (4)$$

4 Type IM: The defects will cause parasitic vias between two layers of the silicon structure. However, the parasitic vias are functionally

1. Since the critical area for vias given defect size x is a function of x^2, equation (1) will yield an infinite value for γ if the size distribution function of [Sta84] is used.

harmful only if the vias occur in places where two conductors overlap. As a result, the conductors are shorted by the pinhole defects. The overlap area can be treated as the critical area for the pinhole defects, assuming: (1) that a pinhole occuring in the overlap area will result in a bridge fault and (2) there is no size distribution for pinhole defects. Therefore, the probability of failure caused by defects of type IM can be estimated by $F_{IM} = \delta o$, where

$$\delta = P_{IM} w^2 \tag{5}$$

According to the above analysis, the parameters P_{OE}, P_{OM}, P_{IE}, P_{IM} and X_0 are process–related, while w and s are determined by the design rules. Since these parameters are independent to routers, the total probability of the failure F of net N can be given by summing up the probabilities of the failures caused by the different types of defects, i.e.

$$\begin{aligned} F &= F_{OE} + F_{OM} + F_{IE} + F_{IM} \\ &= \alpha b + \beta l + \gamma v + \delta o \end{aligned} \tag{6}$$

where α, β, γ and δ are given by the previous equations. It is obvious that the reduction of b, l, v, and o is an effective way to decrease the probability of the failure of net N for a router.

4 New cost function

Given a routing graph $G(V, E)$ with edge weights $\lambda(e)$. The cost of a net is defined as sum of the cost of the edges of the Steiner tree that connects the terminal vertices. Let $E_T \subseteq E$ denote the set of edges, then the cost of a net is given by

$$C = \sum_{e \in E_T} \lambda(e) \tag{7}$$

The goal is to find a minimum cost connection for each net. We combine the conventional cost function of equation (7) with the failure cost function of equation (6) according to

$$C_{new} = C + \varrho F \tag{8}$$

In conventional routing algorithms, the goal is to achieve minimum total net length, implying minimum area. Thus the conventional cost function is modeled as a minimum length cost function. In addition to the net length and the number of vias which are considered in conventional cost functions, the failure cost function introduces two new aspects, namely bridges and overlaps. In essence, minimizing both net length and bridges/overlap is contradictious. Therefore, for dense circuits, net length minimization should be favored over minimizing bridges/overlap because routing space is limited, as opposed to sparse circuits, where minimization of bridges/overlap may be favored over net length minimization. Thus, ϱ is directly proportional to the sparsity of a circuit. We define the sparsity of a circuit as

$$s = 1 - \frac{A_n}{A_r} \tag{9}$$

where A_n denotes the amount of space necessary to lay down all nets as estimated by the global router, and A_r denotes the amount of free routing space after placement. Notice that maximally sparse circuits have $s = 1$ and maximally dense circuits have $s = 0$. Obviously, $s < 0$ indicates circuits that are not routable.

Since ϱ is a weight factor, it depends on the actual values occurring in the conventional cost function C. As we will show in the next section, we can derive a weight factor σ to take into account this dependency. Thus we may write ϱ as

$$\varrho = s\,\sigma \tag{10}$$

5 Incorporating routing style

We assume that the routing space is modelled as a 3–dimensional grid graph $G(V, E)$. An edge $e \in E$ of the grid graph may have one of three directions, called *x*–, *y*– and *v*–*direction*, as indicated in Figure 4(a). Vias are represented by edges in *v*–direction. Wires are allowed to run over edges and bend at grid points. An edge $e \in E$ of the grid graph is said to be *active* if it is part of a wiring pattern. Edges that are not part of a wiring pattern are called *inactive*. The status of an edge may be changed from inactive to active by the router. Possibly, initial wiring patterns exist in the grid graph.

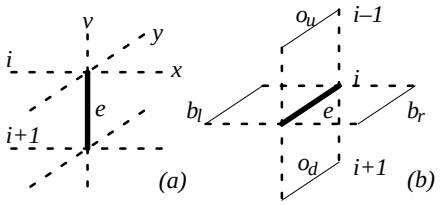

Figure 4 Grid model.

As mentioned in the introduction, we distinguish three aspects that may affect the edge cost function $\lambda(e)$. To cover these aspects, we assume that for each layer i, three costs are specified, namely c_i^x, c_i^y and c_i^v. Here, c_i^x denotes the cost of edges in *x*–direction, c_i^y denotes the cost of edges in *y*–direction and c_i^v denotes the cost of vias connecting layer i and $i+1$. Let $l_i = l_i^x + l_i^y$ denote the total number of edges in layer i for a net, where l_i^x and l_i^y denote the number of edges in *x*–direction and *y*–direction respectively. Furthermore, let v_i denote the number of vias connecting layers i and $i+1$. Then we may write equation (7) as

$$C = \sum_i c_i^x l_i^x + c_i^y l_i^y + c_i^v v_i \tag{11}$$

Since the failure cost function is specific to some material, we assume that for each layer i a failure cost function according to equation (6) is specified, i.e. $F_i = \alpha_i b_i + \beta_i l_i + \gamma_i v_i + \delta_i o_i$. Then, combining the conventional cost function of equation (11) with the failure cost function according to equation (8) yields

$$\begin{aligned} C = \sum_i & (c_i^x + \varrho_i \beta_i) l_i^x + (c_i^y + \varrho_i \beta_i) l_i^y + \\ & (c_i^v + \varrho_i \gamma_i) v_i + \varrho_i \alpha_i b_i + \varrho_i \delta_i o_i \end{aligned} \tag{12}$$

Since the cost of vias are not influenced by any existing wiring pattern, we may discard vias from the following discussion, and set the cost of a via in layer i to $c_i^v + \varrho_i \gamma_i$.

Assume that ϱ is specified for each layer according to $\varrho_i = s\,\sigma_i$, and furthermore assume that the circuit is maximally sparse, i.e. $s = 1$, implying that $\varrho_i = \sigma_i$. Since the circuit is maximally sparse, we want to minimize bridges/overlap.

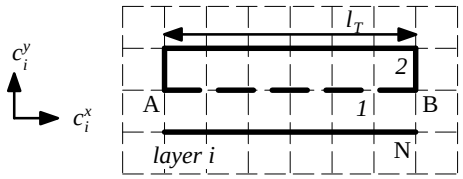

Figure 5 Determination of cost using the new cost function. When min imizing bridges, variant 2 is preferred to variant 1.

In Figure 5, a net N exists in the routing space. Connecting point A and point B, we want the net to follow variant 2 instead of 1, because the criti-

cal area for bridges is minimal for variant 2. Using equation (12) and assuming the length of the net in x–direction is given by l_T, the cost of both variants are given by

$$C_1 = (c_i^x + \sigma_i\beta_i)l_T + \sigma_i\alpha_i l_T$$

$$C_2 = (c_i^x + \sigma_i\beta_i)l_T + 2(c_i^y + \sigma_i\beta_i)$$

using $b = l_T$ for variant 1 and $b = 0$ for variant 2. Since we prefer variant 2 to variant 1, we demand that $C_1 > C_2$ and derive a lower bound for σ_i, i.e.

$$\sigma_i > \frac{2c_i^y}{\alpha_i l_T - 2\beta_i} \tag{13}$$

Similarly, for vertical wires we derive

$$\sigma_i > \frac{2c_i^x}{\alpha_i l_T - 2\beta_i} \tag{14}$$

For overlap we may derive the same functions, only substituting δ_i for α_i, i.e.

$$\sigma_i > \frac{2c_i^x}{\delta_i l_T - 2\beta_i} \text{ and } \sigma_i > \frac{2c_i^y}{\delta_i l_T - 2\beta_i} \tag{15}$$

Combining equations (13), (14) and (15), and setting σ_i to the maximum lower bound yields

$$\sigma_i = \frac{2\ max\ (c_i^x, c_i^y)}{l_T\ min\ (\alpha_i, \delta_i) - 2\ \beta_i} \tag{16}$$

As can be seen from equation (16), σ_i depends on both the cost information per layer and the failure parameters specific to each layer. Parameter l_T may be seen as a threshold net length. If the length by which two nets are in parallel (or overlap) exceeds this threshold, we demand that one of the nets will take a detour as shown in Figure 5.

6 Computing new edge cost

In this section a procedure is given, see Algorithm 1, to determine the final cost of an edge. To be able to do this, the notion of *surrounding edges* is introduced. For each edge $e \in E$ in x– or y–direction, four surrounding edges are identified, denoted as b_l, b_r, o_u and o_d, as indicated in Figure 4(b). The edges b_l and b_r, lying in the same layer as edge e, form the possible bridging edges, while o_u and o_l, lying in respectively the upper and lower layer, form possible overlap edges.

```
procedure determine_edge_cost (i, dir)
begin
  if dir = v then λ := c_i^v + ϱ_i γ_i;
  else
    λ := c_i^dir + ϱ_i β_i;
    if b_l is active then λ := λ + ϱ_i α_i;
    if b_r is active then λ := λ + ϱ_i α_i;
    if o_u is active then λ := λ + ϱ_i δ_i;
    if o_l is active then λ := λ + ϱ_i δ_{i-1};
  fi;
  return λ;
end
```

Algorithm 1: Determination of the new edge cost.

In the above procedure, i is the index of the layer in which edge e lies, and *dir* denotes the direction of the edge, being either x, y or v. For vias no special actions are taken, i.e. if the edge represents a via from layer i to layer $i+1$, the cost λ is set to $c_i^v + \varrho_i\gamma_i$. For all other edges the final cost is influenced by their surrounding active edges. The edge e is assigned the original cost $c_i^{dir} + \varrho_i\beta_i$, plus a cost for each active surrounding edge. The latter depends on the relative position of the surrounding edge with respect to edge e. It is easy to see that this procedure assigns the original edge cost if $s = 0$, implying $\varrho_i = 0$, for all i.

The final edge cost entirely depends on the active edges by which it is surrounded, and therefore may change during routing. To avoid changes in cost due to interaction with already routed segments of the same net, it is assumed that an edge is activated only after all terminals of a net are connected. Notice that the above procedure takes constant time to determine the cost of an edge. Therefore the run time complexity of the original maze router is not influenced by this new cost function.

7 Experiments

The routing approach in which the layout failure mechanism is taken into account has been implemented in the GAS sea of gate layout system [Sle90], using the multi–terminal maze router of [Hui93]. To test the real effect of our new routing strategy, a set of circuits have been designed. Except for mult8 and prim9, all circuits are taken from the MCNC '91 logic synthesis benchmark set. The scales of the layouts range from 150 transistors to 5,000 transistors, while their numbers of nets range from 100 to 3,500. After the placement is finished for each circuit, the sparsity of a layout can be obtained according to the equation (9) presented in section 4. The basic information about the benchmark layouts as well as their sparsities are shown in Table 1.

Table 1: Analysis results.

circuit	# trans	# nets	s %	% change of crit. area OE	OM	IE	IM	ΔLS %
alu2	372	206	78	–23.2	3.9	6.9	2.4	–5.0
apex3	4894	3283	48	–16.4	0.3	3.0	–7.8	–6.4
apla	540	290	77	–23.3	0.6	5.0	2.5	–7.5
bw	504	267	76	–27.2	3.6	9.7	2.4	–7.8
clip	446	242	78	–24.4	1.0	3.9	3.4	–7.7
dk17	328	182	80	–20.0	3.8	4.2	1.8	–4.2
duke2	1206	641	67	–22.1	2.1	4.3	1.3	–6.8
e64	700	429	86	–13.8	0.7	0.0	0.3	–4.0
5xp1	332	181	80	–30.2	2.5	6.1	1.5	–8.8
9sym	658	350	71	–27.6	3.6	5.6	4.3	–7.5
in6	817	455	73	–38.2	4.5	1.2	2.6	–7.9
misex2	564	316	78	–26.7	1.9	4.2	1.7	–7.9
mult8	1566	837	76	–21.4	2.5	3.3	–5.5	–7.5
o64	572	428	86	–14.2	0.6	6.3	–0.1	–4.9
prim9	2112	1167	62	–16.1	3.8	10.5	–8.6	–4.4
radd	146	87	86	–15.5	3.8	12.6	0.5	–3.5
rd84	547	290	75	–25.2	4.0	4.1	2.7	–6.7
sao	526	283	72	–24.3	2.6	3.1	3.5	–7.3
six	358	193	75	–23.4	3.6	10.4	–0.8	–6.2
vg2	245	177	84	–17.8	0.5	3.2	1.7	–5.2

Routing is performed using three layers: a polysilicon layer *ps* and two metal layers *in* and *ins*. Without loss of generality, the parameters α, β, γ, δ are set to 1 and l_T is set to 7. The original edge costs are set according to $c_{ps}^x = 20$, $c_{ps}^y = 3$, $c_{in}^x = 3$, $c_{in}^y = 10$, $c_{ins}^x = 8$ and $c_{ins}^y = 2$, im-

posing a vertical–horizontal–vertical (VHV) routing style. Consequently, for each of the three layers σ can be obtained, i.e. $\sigma_{ps} = 8$, $\sigma_{in} = 4$, and $\sigma_{ins} = 3$.

To compare the results of the conventional router and the proposed routing approach, the benchmark circuits are laid out twice, once using the original routing module of the GAS system and once using the new routing tool. For each circuit the EDAM system [Xue93] is used to obtain the data concerning the failure probability of both layouts.

The critical areas with respect to the four types of faults are computed. The changes in the critical areas as well as the layout sensitivities (ΔLS) are presented in Table 1. From the data, it may be concluded that for all benchmark layouts the critical areas for one layer bridge faults (type OE) decrease 22.6% on average, while the critical areas with respect to one layer open faults only increase 2.5% on average. The critical areas for inter–layer faults, i.e. type IE faults and type IM faults, change very slightly. For the IE faults, this is because via minimization is already considered in the original cost function. Therefore the number of vias will slightly increase since the weight of a via is relatively small in the new cost function. This is because of the extension of the cost function. The changes of the fault IM seem to be random. The reasons are: (1) In the original routing module, the VHV routing style is chosen. Therefore, large area overlap between two metal layers is already prevented by the design style. Obviously, the critical areas caused by the overlaps will not be decreased significantly by putting an extra penalty on them. (2) Since in some cases an increase in overlap between two layers will result in a final decrement of the total cost, it is also possible that the critical areas with respect to these faults will increase.

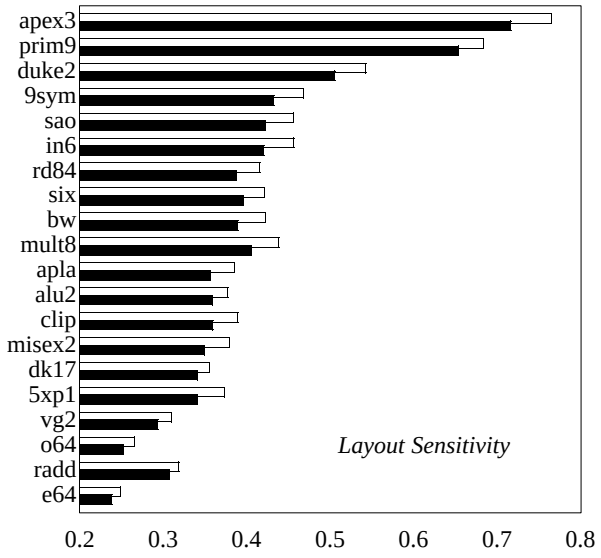

Figure 6 Change in layout sensitivity per circuit.

The total effect of the new routing strategy is shown in the last column in Table 1. According to the data, we find that the layout sensitivities can be decreased 6.4% on average if the failure probability is taken into account in the routing procedure.

Figure 6 shows the sensitivities of the two different layouts per design: white bars represent the sensitivities of the layouts made by the original router and black bars indicate the sensitivities of the layouts made by the new routing module.

8 Conclusions

In this paper a novel routing strategy producing layouts that are less susceptible to spot defects has been presented. Based on an analysis of spot defects, the four types of the main random disturbance in IC processes are modelled. A formula indicating the failure probabilities of these faults is derived. Combining the failure cost function with the conventional cost function, a new cost function for the general routing problem is devised. By using this new cost function, a good trade–off between the minimization of the total net length and the maximization of the manufacturability of a layout can be obtained. The experimental data show that even for very dense circuits the layout sensitivities can be significantly decreased by the proposed routing approach while the layout areas are kept the same.

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