Hierarchical Optimization Methodology for Wideband Low Noise Amplifiers

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Abstract— In this paper, we present a systematic synthesis methodology for fully integrated wideband low noise amplifiers that simultaneously optimizes impedance matching, noise figure, and other performance parameters. Leveraging an accurate analytical model, we hierarchically couple global optimization techniques with local convex optimization methods to efficiently locate optimal wideband LNA circuits. The results indicate that the methodology yields significant improvement in key LNA design constraints over existing methodologies while achieving up to one order of magnitude speedup in computational performance.

I. Introduction

Wideband wireless systems will provide the bandwidth necessary to significantly increase performance and decrease power consumption to meet the growing demand for more powerful wireless applications with greater functionality. Low noise amplifiers (LNA) play a vital role in determining the performance, power consumption, and reliability of the RF receiver [1]. For wideband applications, LNAs must be designed for input and output impedance matching, which facilitates maximum power transfer, low noise, and sufficiently flat gain across the entire range of operating frequencies. In addition to these important design considerations, fully integrated wideband LNA designs must also consider the impact of circuit element sizing for system-on-chip (SoC) integration and the parasitics that are inherently present in the mixed-signal environment.

Given the increasing demand for wireless systems in SoC technology, the automated design and optimization of fully integrated CMOS LNAs is vital for meeting power, performance, and yield requirements while substantially reducing time-to-market and cost [2,3]. Previous techniques for designing wideband LNAs utilize analytical expressions for the LNA design parameters, such as device width and passive component values, that optimize certain figures of merit [1, 4–10]. Due to the simplifying assumptions necessary to create the explicit expressions, these techniques may not account for the inductor or device parasitics and typically lack the flexibility to constrain component values to ensure that the circuit can be fully integrated on-chip. In contrast, design techniques based numerical optimization can systematically locate optimal designs that simultaneously meet system requirements while restricting component values to those suitable for SoC integration.

In this paper, we develop a systematic methodology to optimize and synthesize wideband LNAs. Leveraging an accurate circuit model, we hierarchically couple global optimization techniques with local convex optimization methods to efficiently locate optimal wideband designs. To improve the performance of the methodology, we dynamically adjust the complexity of the circuit models during the optimization process. The results indicate that the hierarchical methodology yields significant improvement in key LNA design constraints over existing equation-based methodologies while achieving up to one order of magnitude speedup in computational performance. Leveraging the efficiency of our synthesis methodology, we are able to generate Pareto surfaces for key design trade-offs in minutes.

II. Wideband LNA Modeling

Wideband LNA circuits based on the inductively degenerated cascode topology that utilize Butterworth or Chebyshev filters for the input impedance matching network have demonstrated the potential for excellent impedance matching, noise figure, power consumption, and gain across the entire wideband frequency range [1, 6, 10]. Therefore, we consider the filter-based LNA topology depicted in Figure 1. To accurately characterize the input and output impedance matching, noise figure, power dissipation, and gain of fully integrated wideband LNAs, we have developed an analytical model that captures the effect of transistor parasitics, the internal resistances of the inductors, and the biasing circuitry. Despite its increased complexity, the accuracy of the proposed model makes it well-suited for numerical LNA optimization.

A. Optimization of Passive Components

Integrated inductors and capacitors are required in LNA designs in order to match the input and output impedances of the amplifier. Among passive components, integrated spiral inductors typically have the lowest quality factors, and consequently, the impact of their parasitics are significant for impedance matching and noise figure [1]. At a particular frequency, an equivalent resistance, $R_{eff} = \omega L_{eff}/Q$, where Q and L_{eff} are the inductor's quality factor and effective inductance [11], can capture the impact of on-chip inductor parasitics. R_{eff} and L_{eff} are not just the physical inductance and resistance of

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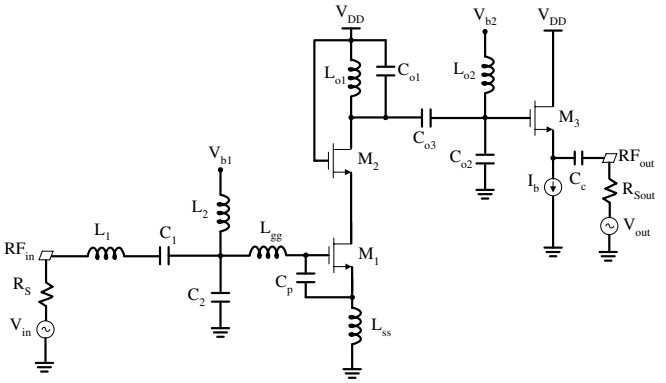

Fig. 1. Wideband inductive source degenerated cascode LNA topology.

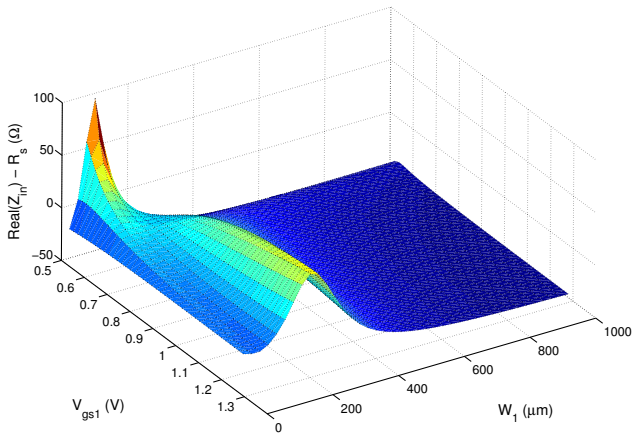

Fig. 2. Real(Z_{in}) minus R_s versus W_1 and V_{gs1}. Note that the constraint function has multiple convex sets.

the spiral inductor's conductors, but also include the effects of all resistive, capacitative, and inductive parasitics in the substrate and conductors [11, 12]. Since our wideband synthesis methodology evaluates the performance parameters at a several discrete frequencies, the R_{eff} values at each frequency can accurately characterize the behavior of on-chip inductors in wideband LNAs. However, for time-domain simulation or characterization at multiple frequencies using a circuit-level simulator, wideband inductor models based ladder circuits or the 2-π configuration should be used [13, 14]. For the modeling and design integrated metal-insulator-metal (MIM) capacitors, we utilize the techniques presented in [15].

Since our LNA synthesis methodology requires the repeated evaluation of many inductor designs with different inductance values, optimizing each inductor's geometry during each iteration of the LNA synthesis process would be prohibitively expensive. Instead, we utilize the synthesis technique presented in [16] to generate a surrogate function ($Q_{max} = S(L_{eff}, f_o, f)$) to determine the optimal quality factor (Q_{max}) for a given frequency at which the quality factor is maximized (f_o), operating frequency (f), and L_{eff} value. We constrain the minimum self-resonant frequency to 15 GHz to ensure that the inductors are operating in the inductive regime for all frequencies in the wideband range. Once the final LNA design is produced, the geometric dimensions of the integrated inductors can be determined using an inductor optimization method [17].

B. Noise Figure

The noise figure is typically the most important figure of merit for the LNA. The noise figure model captures device and passive component parasitics and short channel noise sources such as gate induced noise, distributed gate resistance, and channel resistance [18, 19]. To calculate the noise figure, we divide the output current into terms that capture the relevant signal and noise current sources, which can be expressed as

$$i_{(M2)} = i_{ss} + i_{sn} + i_{in} + i_{m1n} + i_{m2n} \qquad (1)$$

where i_{ss} and i_{sn} are the current contributions from the source signal and noise, i_{in} is the input network noise current, i_{m1n} is the noise current generated from M_1, and i_{m2n} is the noise current generated from M_2. The noise figure (NF) is expressed as the ratio between the total output noise power and the output noise power generated by the source internal resistance. By dividing the NF according to its constituent noise sources, it can be expressed as

$$NF = 1 + NF_{I/Pnet} + NF_{M1} + NF_{M2} \qquad (2)$$

where $NF_{I/Pnet}$, NF_{M1}, and NF_{M2} are the noise generated by the input impedance matching network, M_1, and M_2, respectively, which are determined using wideband models based on [20, 21].

C. Other Design Parameters

To capture the parasitics of passive components and devices in the LNA, we developed and implemented a generalized impedance matching model. Despite its increased complexity, the accuracy of the proposed models makes it well-suited for numerical LNA synthesis. The model considers the effect of device parasitics such as C_{gd}, C_{db}, C_{sb}, and R_m [20] as well as the parasitic resistances of the inductors as described in Section II-A. We have developed an input and output impedance matching formulation as well as a gain model using the methodology presented in [20, 20]. For power dissipation, we use the model from [22]. Leveraging the analytical model, we can optimize and synthesize fully integrated CMOS LNAs to meet performance requirements while ensuring that passive components are suitable for on-chip integration.

D. Design Space Analysis

Design problems solved using gradient-based nonlinear constrained optimization techniques must have convex objective and constraint functions to guarantee that the algorithms will converge to the global solution. To explore the convexity of the design space, we examined the noise figure, input and output impedance matching, gain, and power dissipation for a typical wideband LNA design. Our results indicate that the noise figure, gain, and power consumption are convex with respect to both the transistor variables and passive components values. However, the input and output impedance matching constraint

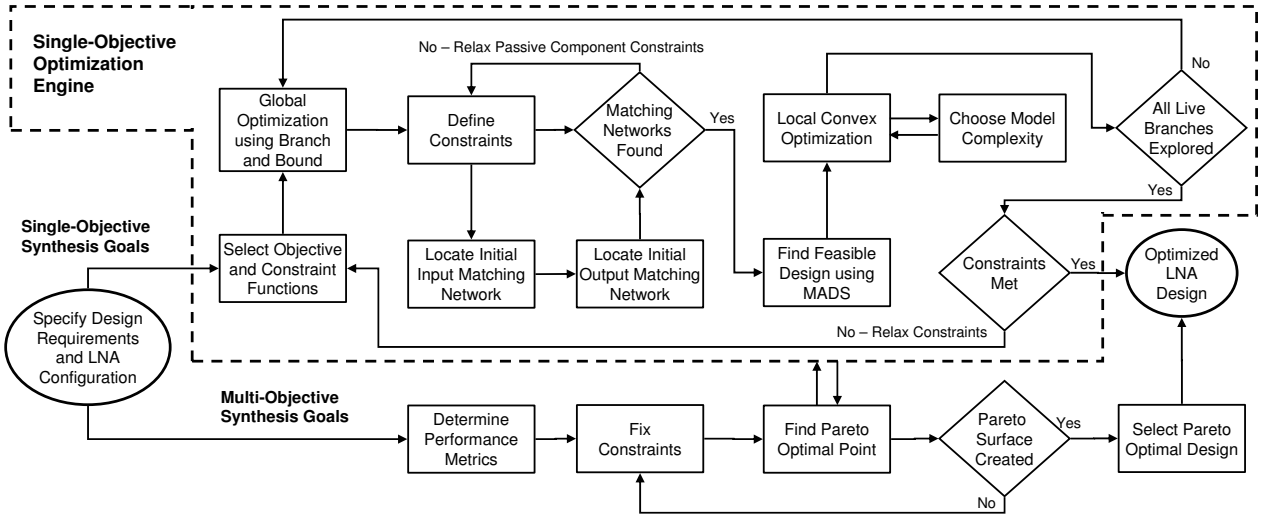

Fig. 3. The wideband LNA synthesis methodology.

functions have multiple convex sets with respect to the design parameters. Figure 2 depicts the real part of Z_{in} minus R_s versus W_1 and V_{gs1} at 3.1 GHz. The multiple convex sets are due to the parasitic capacitances in M_1 resonating with different passive component values as W_1 is varied. Therefore, gradient-based constrained optimization techniques alone may potentially converge to sub-optimal or infeasible points when the optimization algorithm starts at certain locations in the design space.

III. Optimization and Synthesis Methodology for Wideband LNAs

A. LNA Optimization Problem Formulation

To systematically realize fully integrated LNAs for wideband applications, we have developed a variability-aware hierarchical optimization and synthesis methodology. In general, the multi-objective LNA optimization problem can be formulated as

$$\begin{aligned} \text{Minimize} \quad & \begin{bmatrix} \overrightarrow{F}\left(\overrightarrow{x},\overrightarrow{f}\right) \\ \overrightarrow{G}\left(\overrightarrow{x},\overrightarrow{f}\right) \\ \overrightarrow{P}\left(\overrightarrow{x}\right) \end{bmatrix} \\ \text{Subject to} \quad & \begin{pmatrix} (\overrightarrow{Z_{in}}(\overrightarrow{x},\overrightarrow{f})) \leq (Z_{sin}) \\ (\overrightarrow{Z_{out}}(\overrightarrow{x},\overrightarrow{f})) \leq (Z_{sout}) \\ \overrightarrow{x_{min}} \leq \overrightarrow{x} \leq \overrightarrow{x_{max}} \end{pmatrix} \end{aligned} \tag{3}$$

$$\overrightarrow{x} = \left[W_1, W_2, W_3, V_{gs1}, V_{gs3}, \overrightarrow{Z_{ic}}, \overrightarrow{Z_{oc}}\right]^T \tag{4}$$

$$\overrightarrow{f} = [f_{min}, f_2, \cdots, f_{n-1}, f_{max}]^T \tag{5}$$

where $\overrightarrow{F(\overrightarrow{x})}$, $\overrightarrow{G(\overrightarrow{x})}$, and $\overrightarrow{P(\overrightarrow{x})}$ are the noise figure; negative gain, since gain should be maximized; and power consumption of the LNA, respectively. The vector $\overrightarrow{x}$ contains the LNA design parameters, where $\overrightarrow{Z_{ic}}$ and $\overrightarrow{Z_{oc}}$ are vectors of inductor, capacitor, and resistor component values for the input and output impedance matching networks, and Z_{sin} and Z_{sout} are the maximum worst-case input and output source impedances that need to be matched. Typically less than 5 frequency points are required to ensure relatively flat impedance matching and gain across the frequency range of interest. The bound constraints on the passive component values are used to ensure that the optimized LNA design can be fully integrated on-chip. Since $\overrightarrow{F(\overrightarrow{x})}$, $\overrightarrow{G(\overrightarrow{x})}$, and $\overrightarrow{P(\overrightarrow{x})}$ cannot be simultaneously minimized, we need to find the Pareto-optimal surfaces relating each of these design metrics to synthesize an LNA that exploits performance trade-offs.

B. Single-Objective LNA Optimization

Solving the multi-objective optimization problem presented in (3) typically requires the solution to a series of single-objective LNA design problems. For noise figure minimization, this single-objective optimization problem would be cast as

$$\begin{aligned} \text{Minimize} \quad & \| \overrightarrow{F}\left(\overrightarrow{x},\overrightarrow{f}\right) \|_2 \\ \text{Subject to} \quad & \begin{pmatrix} \overrightarrow{Gain}\left(\overrightarrow{x},\overrightarrow{f}\right) \geq G_{min} \\ \overrightarrow{Gain}\left(\overrightarrow{x},\overrightarrow{f}\right) \leq G_{max} \\ \overrightarrow{P}\left(\overrightarrow{x}\right) \leq P_{max} \\ (\overrightarrow{Z_{in}}(\overrightarrow{x},\overrightarrow{f})) \leq (Z_{sin}) \\ (\overrightarrow{Z_{out}}(\overrightarrow{x},\overrightarrow{f})) \leq (Z_{sout}) \\ \overrightarrow{x_{min}} \leq \overrightarrow{x} \leq \overrightarrow{x_{max}} \end{pmatrix} \end{aligned} \tag{6}$$

where $\overrightarrow{Gain}$ is the gain of the LNA, G_{min} is the minimum allowed gain, G_{max} is the maximum allowed gain, and P_{max} is the maximum allowed power dissipation. The rest of the variables are defined in Section III-A. By taking the 2-norm of the noise figures at different frequencies, we ensure that the overall value of F is minimized over the entire operating frequency range. We set lower and upper limits on the gain to ensure that it remains relatively flat across the frequency range.

We must develop and employ optimization techniques that exploit the aforementioned design space characteristics.

Stochastic optimization routines based on simulated annealing [23], particle swarm optimization [24], or evolutionary algorithms [25], while eventually converging to near-optimum solutions, require significant simulation time for problems with nonlinear constraints. Consequently, these algorithms are appropriate for complex optimization problems with noisy objective and constraint functions with many local minima or discrete design variables. Based on (6) and Figure 2, the wideband LNA design space does not exhibit these characteristics, and therefore, the significant computational cost of stochastic optimization routines cannot be justified.

Optimization routines based gradient-based nonlinear programming techniques can provide a substantial performance improvement over stochastic optimization. However, since the design space contains multiple convex sets, using gradient-based nonlinear programming techniques alone may produce sub-optimal results or fail to find feasible solutions. Therefore, we have developed a hierarchical optimization methodology that combines global and local convex optimization methods. Global optimization based on branch and bound dynamically segments the design space to find feasible convex sets that gradient-based local optimization can efficiently explore [26]. To solve the local convex optimization problem, we utilize Sequential Quadratic Programming (SQP), a nonlinear programming technique that exploits the gradients of the objective and constraint functions to accelerate convergence [17]. Our computed Pareto surfaces and their favorable comparison with the Monte Carlo simulation of random designs depicted in Figure 6 and described in Section IV-B empirically confirm that we are able to successfully generate optimal LNAs using the proposed hierarchical optimization methodology.

C. Overall Synthesis Methodology

Figure 3 depicts the overall wideband LNA synthesis methodology. If we want to generate the Pareto surfaces analyzing the trade-off between performance metrics, we utilize the ϵ-constraint method [16], which forms the Pareto surface by solving a series of single objective optimization problems for each set of constraint values for a particular objective. Our single objective optimization engine is utilized during either during each iteration of Pareto optimization or for LNA synthesis with fixed design constraints. The branch and bound algorithm to determine the intervals for the local convex optimization process. We first locate feasible initial input and output impedance matching networks in order to accelerate convergence by using SQP on the following optimization problem:

$$\begin{aligned} \text{Minimize} \quad & \| \operatorname{Re}(Z_{in}(\overrightarrow{Z_{ic}}, \overrightarrow{f})) - \operatorname{Re}(Z_{sin}) \\ & + \operatorname{Im}(Z_{in}(\overrightarrow{Z_{ic}}, \overrightarrow{f})) - \operatorname{Im}(Z_{sin}) \|_2^2 \\ \text{Subject to} \quad & \overrightarrow{Z_{ic,min}} \leq \overrightarrow{Z_{ic}} \leq \overrightarrow{Z_{ic,max}} \end{aligned} \tag{7}$$

where Z_{in} is the input impedance of the LNA, and $\overrightarrow{Z_{ic,min}}$ and $\overrightarrow{Z_{ic,max}}$ are the minimum and maximum inductor and capacitor values for the input impedance matching network. We utilize an optimization formulation similar to (7) to find a feasible start point for the output matching network. Once feasible input and output matching networks for the initial transistor parameters are obtained, we then optimize the LNA using a single-objective version of the problem formulated in (3) for the specified performance objectives and constraints using SQP. If the performance constraints cannot be met, we relax the constraints on passive components based on their quality factor surrogate functions.

To improve the performance of the synthesis methodology, we dynamically vary the complexity of the modeling techniques during the optimization process. When far from the solution, we do not calculate impact of inductor parasitics and the transistor M_2 on noise figure, impedance matching, and gain. Once the directional derivative of the solution and maximum constraint violation reach a certain threshold, we switch to the more complex modeling methodology that includes the affect of inductor parasitics and all of the transistors in the circuit. The hierarchical modeling scheme results in significant computational savings when optimizing and synthesizing wideband LNAs.

IV. Results

A. Design Examples

To evaluate our wideband LNA synthesis methodology, we perform single-objective LNA optimization using the formulation described in (6) for three design examples that demonstrate the efficacy of the methodology. For all three design examples, we assume that the wideband LNA is fabricated in the TSMC $0.18\mu m$ mixed-model process and enforce the following constrains on the design parameters: $W_1, W_2, W_3 \in [20, 1000]$ μm, $V_{gs}, V_{gs3} \in (V_T, V_{dd} - V_T)$, inductors $\in [0.01, 5]$ nH, and capacitors $\in [0.05, 2]$ pF. We constrain the upper bound of the inductors and capacitors to 5 nH and 2 pF, respectively, to ensure on-chip integration of the passive components. For the integrated inductors, we assume that top metal layer is 2 μm thick and that the substrate has a low conductivity ($\sigma \ll 100(\Omega \cdot m)^{-1}$). We also assume 50 Ω for input and output source impedances.

For design example 1, we synthesize a wideband LNA using the circuit topology displayed in Figure 1 with -10 dB input and output matching constraints and minimize the noise figure over the frequency range of 2.5 to 7.0 GHz. Figure 4 displays the noise figure and impedance matching results from Cadence Spectre RF, a circuit level-simulator, for design example 1. The S-parameter analysis for two-port network is used to simulate input matching (S11) and output matching (S22), while S-parameter noise analysis is used to simulate the noise figure. The CMOS model used is BSIM3v3 0.18 μm from TSMC, with an integrated noise model, short channel effects, and a non-quasistatic assumption for the internal parasitics of the transistors. The minimum noise figure is 1.9 dB, while both the in-band input and output impedance matching are less than -12 dB. The analytical model results, which are depicted in Table I, closely match the results from Spectre RF.

In design example 2, we enforce an additional maximum power dissipation constraint of 10 mW on the problem solved in design example 1 and increase the frequency range to 3.1 to 10.6 GHz, which is the ultra-wideband frequency range described in [1]. Figure 5 displays the noise figure and impedance matching results from our analytical model for design example 2. Note that the additional power dissipation constraint

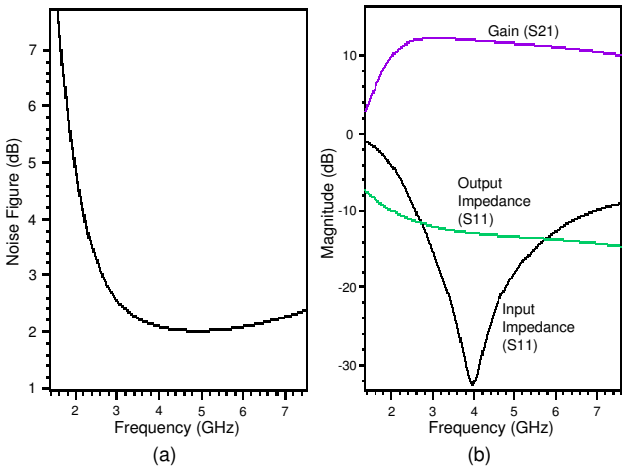

Fig. 4. Spectre RF results for (a) noise figure, (b) gain (S_{21}), and input (S_{11}) and output (S_{22}) matching for example 1.

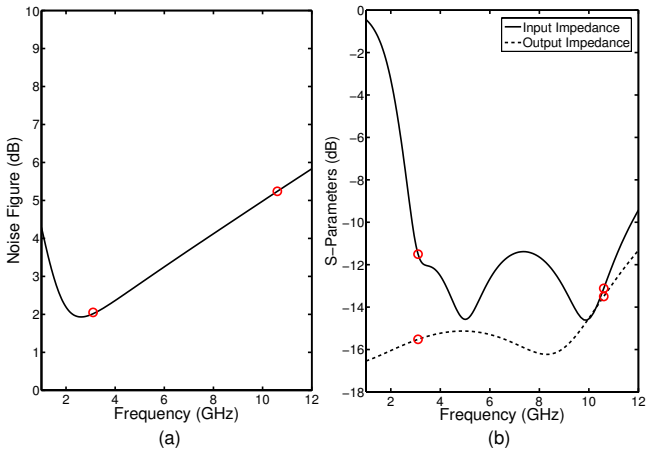

Fig. 5. Noise figure (a) and input and output matching (b) for example 2.

TABLE I
INPUT IMPEDANCE MATCHING AND NOISE FIGURES OBTAINED FROM THE HIERARCHICAL OPTIMIZATION METHODOLOGY AND AN EXISTING EQUATION-BASED DESIGN TECHNIQUE.

	Worst-Case Input Matching		Minimum Noise Figure	
Example	Hierarchical Optimization	Analytical Design	Hierarchical Optimization	Analytical Design
1	-10.0 dB	-0.7 dB	1.9 dB	1.9 dB
2	-11.4 dB	-1.7 dB	2.0 dB	2.2 dB
3	-9.0 dB	-3.5 dB	1.3 dB	1.8 dB

TABLE II
NUMBER OF MODEL EVALUATIONS FOR OUR HIERARCHICAL MODELING TECHNIQUE AND FULL-COMPLEXITY MODELING.

	Hierarchical Modeling		Standard Modeling		
Example	Simple	Complex	Simple	Complex	Speedup
1	9096	1938	0	10525	2.7
2	10880	856	0	24762	11.3
3	11242	1963	0	25090	5.5

increases the noise figure over the values obtained in design example 1. We also simulated example 2 in Spectre RF and found that the results closely match the analytical model with a IIP3 linearity of -2.87 dBm at 3.1 GHz. In the final design example, we enforce a maximum power dissipation constraint of 15 mW, a minimum gain of 10 dB, and an input and output impedance matching constraint of -8 dB over an operating frequency range of 3.1 to 5.1 GHz, which has been proposed for some wideband applications [9]. The noise figure ranges from 1.3 to 1.8 dB in the passband, while both the in-band input and output impedance matching are less than -9 dB. The gain ranges from 10 to 14 dB. Despite the additional gain constraint, the narrower bandwidth allows the methodology to produce a design with a lower noise figure than in the 3.1 - 10.6 GHz case.

For the three design examples, we compare our optimization and synthesis methodology with the analytical design technique presented in [1]. Table I lists the results for the comparison. In each of the three design examples, using an analytical design technique that does not account for passive component parasitics and short channel effects yields circuits with poor input impedance matching, with a 93 percent degradation in design example 1. In terms of noise figure, our methodology provides a 38 percent improvement.

Using the hierarchical modeling technique presented in Section III-C, we significantly improve the computational performance of the synthesis methodology. Table II displays the number of model evaluations for our hierarchical modeling technique and standard full-complexity modeling. In design example 2, hierarchical modeling required 10,880 evaluations of the low-complexity analytical model and 856 evaluations for the full-complexity analytical LNA model with a total CPU runtime of 38.6 seconds. In contrast, optimizing the design without hierarchal modeling requires 24,762 evaluations of the full-complexity analytical LNA model with a CPU runtime of 438.1 seconds. Therefore, the hierarchical modeling approach provides up to an 11.3 speedup in the optimization process.

B. Pareto Optimization

In order to locate wideband LNA designs that provide the appropriate design constraints that maximize critical performance metrics for a particular application, the generation of Pareto-optimal trade-off surfaces is crucial. We generated the Pareto surface comparing noise figure versus power dissipation for frequency points in the wideband range, which is depicted in Figure 6. From the Pareto surface, it is clear that increasing the power consumption beyond 20 mW only yields limited improvement in noise figure.

To validate our synthesis methodology, we performed a Monte Carlo simulation of 1,000 LNA design with random W_1, W_2, and V_{gs} values and input and output impedance networks matched using the formulation in (7). The noise figure/power dissipation performance combinations of all of the randomly simulated designs are dominated by the calculated Pareto surface, which demonstrates that our methodology is closely approximating the Pareto surface. Therefore, the hierarchical wideband LNA optimization engine is locating op-

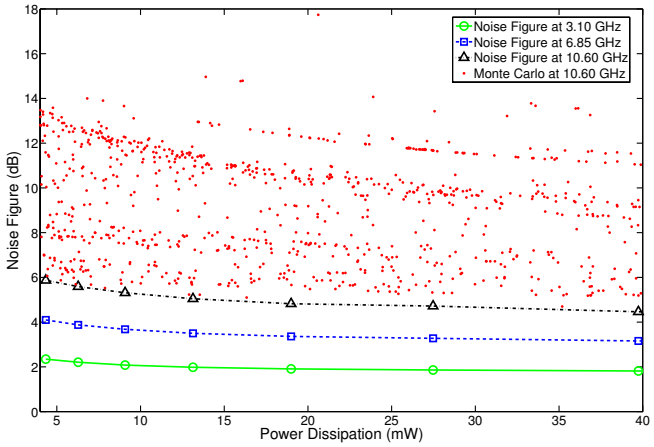

Fig. 6. Pareto surfaces for noise figure versus power dissipation at 3.10, 6.85, and 10.60 GHz. The Monte Carlo simulations reveal that the synthesis methodology is producing optimal designs.

timal designs. Using the information from the Pareto-optimal performance surface, the designer or design automation tools can make informed decisions on how to trade-off key LNA performance requirements.

V. Conclusion

The systematic numerical optimization methodology for fully integrated wideband LNAs simultaneously optimizes impedance matching, noise figure, and other performance parameters by hierarchically coupling global optimization with convex local optimization methods. The results indicate that the hierarchical methodology yields significant improvement in key LNA design constraints over existing equation-based methodologies while achieving up to one order of magnitude speedup in computational performance. Given the increasing demand for wireless systems in SoC technology, our synthesis methodology will enable the rapid realization of fully integrated wideband CMOS LNAs.

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