

CS Seminar Series

Title: Looking "Up" for Technology Scaling

Speaker: Puneet Gupta (UCLA)

Date: Friday April 19, 11 am-12 pm

Location: DBH 6011

Abstract:

Scaling of physical dimensions faster than the optical wavelengths or equipment tolerances used in the manufacturing line has led to increased process variability and low yields which make manufacturing expensive and design unpredictable. "Equivalent scaling" improvements - perhaps as much as one full technology generation, can come from looking "up" to circuit design and even to software (operating systems, compilers and applications).

In first half of the talk, I will talk about design-assisted technology scaling. With few examples from the lithographic patterning, and mask flows, I will illustrate how design information can be leveraged practically to radically reduce pessimism inherent in semiconductor manufacturing as well as guide process research and development.

In the second half of the talk, I speculatively argue for underdesigned and opportunistic computing machines which offload some of the variability handling burden to higher layers in the hardware-software stack. With examples, I will show that a fluid hardware-software interface can result in substantial improvements in power, yield and application quality.

Bio:

Puneet Gupta (<http://nanocad.ee.ucla.edu>) is currently a faculty member of the Electrical Engineering Department at UCLA. He received the B.Tech degree in Electrical Engineering from Indian Institute of Technology, Delhi in 2000 and Ph.D. in 2007 from University of California, San Diego. He co-founded Blaze DFM Inc. (acquired by Tela Inc.) in 2004 and served as its product architect till 2007.

He has authored over 100 papers, 16 U.S. patents, a book and a book chapter. He is a recipient of NSF CAREER award, IBM Faculty Award, ACM/SIGDA Outstanding New Faculty Award, European Design Automation Association Outstanding Dissertation Award and SRC Inventor Recognition Award. Dr. Puneet Gupta has given tutorial talks at DAC, ICCAD, Intl. Conference on Microelectronic Test Structures, SPIE Advanced Lithography Symposium, etc. He served as the Program Chair of IEEE DFM&Y Workshop 2009, 2010, 2011. He currently leads the multi-university IMPACT+ Center (<http://impact.ee.ucla.edu>) which looks at design and process challenges for future semiconductor technologies.

Dr. Gupta's research has focused on building high-value bridges across application-architecture-implementation-fabrication interfaces for

lowered cost and power, increased yield and improved predictability of integrated circuits and systems.

Host: Eli Bozorgzadeh, Associate Professor, Computer Science Department