Center for Embedded Computer Systems
University of California, Irvine

CS Seminar Series

"The Delft Reconfigurable VLIW Processor"

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Abstract

In this presentation, we present the rationale and design the Delft reconfigurable and parameterized VLIW processor called rho VEX (rVEX in short). Its architecture is based on the Lx/ST200 ISA developed by HP and STMicroelectronics. We implemented the processor on an FPGA as an open-source softcore and made it freely available. Using the rVEX, we intend bridge the gap between general-purpose and application-specific processing through parametrization of many architectural and organizational features of the processor. The initial set of parameters include: instruction set (number and type of supported instructions), the number and type of functional units (FUs), issue-width (number of slots), register file size, memory bandwidth. The parameters can be set in a static or dynamic manner in order to provide the best performance or the best utilization of available resources on the FPGA. A complete toolchain including a C compiler and a simulator is freely available. Any application written in C can be mapped to the rVEX processor. This VLIW processor is able to exploit the instruction level parallelism (ILP) inherent in an application and make its execution faster compared to a RISC processor system. Recent developments will be presented. The rVEX is currently being further developed within an EU-funded project called ERA: Embedded Reconfigurable Architectures.

Finally, we will present the ERA project. The starting point of the ERA project is the observation that the complexity and diversity of embedded systems is rising and causing extra pressure in the demand for performance at the lowest possible power budget. Consequently, designers face the challenge brought by the power and memory walls in the production of embedded platforms. The focus of the ERA project is to investigate and propose new methodologies in both tools and hardware design to break through these walls and help design next-generation embedded systems platforms. The proposed strategy is to utilize adaptive hardware to provide the highest possible performance with limited power budgets. The envisioned adaptive platform employs a structured design approach that allows integration of varying computing elements, networking elements, and memory elements. More details on the project together with recent developments and results of the project will be presented.

Biography

Stephan Wong received his PhD in Computer Engineering from the Electrical Engineering, Mathematics and Computer Science faculty of the Delft University of Technology (TU Delft), The Netherlands, in December 2002. He is currently working as an associate professor at the Computer Engineering Laboratory at the Delft University of Technology (TU Delft), The Netherlands. He has considerable experience in the design of embedded reconfigurable media processors. He has worked also on microcoded FPGA complex instruction engines and the modeling of parallel processor communication networks. His research interests include embedded systems, multimedia processors, complex instruction set architectures, reconfigurable and parallel processing, microcoded machines, and distributed/grid processing. He has served in many conference and workshop PCs as well as participated in the organization of many conferences as PC chair, general chair, or other chair positions and was editor of several proceedings and journals. He is currently coordinator of an EU project in the FP7 framework: Embedded Reconfigurable Architectures (ERA). He is a senior member of the IEEE and member of the ACM and Hipeac NoE. Visit http://www.ce.ewi.tudelft.nl/wong/ for a more up-to-date overview of all his activities.

Tuesday, March 26, 2013
2:00-3:00PM
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