A New Method to Improve Accuracy of Leakage Current Estimation for Transistors with Non-Rectangular Gates due to Sub-wavelength Lithography Effects

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***Abstract*–Non-ideal pattern transfer from drawn circuit layout to manufactured nanometer transistors can severely affect electrical characteristics such as drive current, leakage current, and threshold voltage. Obtaining accurate electrical models of non-rectangular transistors due to sub-wavelength lithography effects is indispensable for DFM-aware nanometer IC design. In this paper, TCAD device simulations are utilized to quantify the accuracy of a standard equivalent gate length extraction approach for non-rectangular transistors. It is verified that threshold voltage and current density are non-uniform along the channel width due to narrow-width related edge effects, leading to significant inaccuracy in the sub-threshold region. A new EGL extraction method utilizing location-dependent weighting factors and convex parameter extraction techniques is proposed to account for the current density non-uniformity. Preliminary results verified by TCAD simulations indicate that the accuracy of leakage current estimation for non-rectangular transistors can be significantly improved. The method is readily applicable to calibration with real silicon data.**

I. INTRODUCTION

Following Moore's Law, the critical dimension (CD) of integrated circuits has shrunk to sub-wavelength regime of optical lithography, i.e., the critical dimension is close to or smaller than the exposure wavelength. Lithographic patterning distortions due to effects such as optical diffraction, lens aberration, and polarization, are no longer negligible. Even with resolution enhancement techniques, manufactured nanometer transistors can still suffer from serious gate shape pattern distortion. Obtaining accurate transistor models to account for across-gate critical dimension variation is indispensable for electrically DFM-aware circuit design closure [16]. Current BSIM models adopted by SPICE simulators cannot incorporate non-rectangular pattern distortion partly because threshold voltage and leakage current have complex nonlinear relationship with gate shape. Ideally, one may utilize calibrated 3D TCAD transistor simulations and SPICE parameter extraction for post-lithography electrical performance verification of each transistor. It is usually computationally prohibited when each transistor has different shape distortion.

There have been several more computationally viable approaches to model non-rectangular transistors based on shape information, standard compact transistor models, and SPICE simulations. In earlier works which can be traced back to [1][2], each non-rectangular gate is decomposed into a number of rectangular slices. Each slice is modeled as an independent MOSFET with own channel length (L) and channel width (W). The MOSFET with non-rectangular gate is then represented by a number of narrower rectangular MOSFETs connected in parallel. This approach may involve with several issues: (a) It increases circuit transistor counts and hence simulation time, (b) standard transistor models may not be available for transistors with length smaller than the minimum length allowed in BSIM models, (c) the sampling resolution (slice width) is limited by the minimum allowable width, and (d) actual current density distribution with non-rectangular channels may not be well represented by the narrower transistors due to different boundary conditions.

To resolve some of these issues, a standard equivalent gate length (EGL) extraction method was first proposed in [9] and applied in [11]. It translates a number of lengths and widths of rectangular slices that make up the non-rectangular gate shape into one equivalent rectangular transistor with an effective gate length as shown in Fig. 1. The effective channel length is based on summing up the current through each slice. Drive current (I_{on}) is used to extract on-state EGL for delay analysis, and leakage current (I_{off}) is used to extract off-state EGL for static power analysis. The difference should not be a concern as different analysis tools are used. Each slice current is calculated from the current density of a flat or very wide transistor with the slice length, to minimize boundary effects.

However, narrow-width related edge effects caused by the fringing capacitance due to line-end extension, dopant scattering due to STI edges [4], and well proximity effects (WPE) [7] can result in device threshold voltage and current density variations along the channel width. In [10], a location-dependent threshold voltage (V_{th}) model was proposed to take into account these effects. It has been shown that I_{off} depends not only on the magnitude of length variation, but also on its location along the device width. Fitting the V_{th} model involves

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with extracting coefficients from quadratic polynomials whose exponential is integrated. In [13], similar method accounting for this location dependency was proposed by translating the shift in effective V_{th} at the edges to the shift in effective length of the gate at the edges. The EGL can be a continuous function of gate-source voltage (V_{gs}) to extrapolate intermediate values of length between the off and on states.

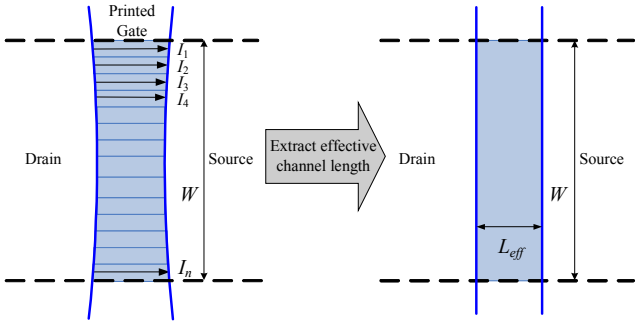


Fig. 1. Approximate a non-rectangular transistor to a rectangular transistor with an effective channel length.

In this paper, we examine the impact of the narrow-width related edge effects on electrical characteristics of transistors and verify the accuracy of the standard EGL method by TCAD device simulation in Section II.B and II.C respectively. In Section III.A, we propose a new EGL extraction method with location-dependent weighting factors to improve the accuracy of the leakage current (I_{off}) estimation. These weighting factors can be easily integrated into the standard EGL extraction procedure of [9], and their unique globally optimal values can be found efficiently by convex parameter extraction techniques, which may provide certain advantages. In Section III.B, we demonstrate the extraction procedure with eight different non-rectangular gate shapes. A separate non-rectangular gate shape is used for cross-validation to demonstrate its effectiveness. TCAD simulations indicate that it is capable of improving the accuracy of the leakage current estimation significantly.

II. Device Simulation

ISE DESSIS device simulator [6] is used to estimate impacts of the narrow-width related edge effects on device characteristics, and to verify accuracy of the standard EGL extraction method. A fictitious TCAD model of a 90-nm transistor is built, with a list of device parameters summarized in Section II.A. In Section II.B, we compare 2D with 3D device simulations to characterize the impacts of the narrow width effects on the I_{on} and I_{off} when the gate is perfectly rectangular, i.e., when lithographic distortion is neglected. In Section II.C, we verify the results of the standard EGL extraction method with 3D TCAD simulation on a fictitious non-rectangular 90-nm transistor resulted from severe lithographic patterning distortion.

A. Device Simulation Setup

A N-channel MOSFET 3D TCAD device model used in the following simulations is calibrated to the 90-nm Predictive Technology Model [14]. Initial device boundaries and doping profiles are defined based on its BSIM4 process parameters. They are then tuned to match I-V characteristics as closely as possible. Final parameters used are summarized in TABLE I.

TABLE I
TCAD PARAMETERS USED FOR A N-CHANNEL MOSFET

Parameters	Description	Value
L	Channel length	90 nm
W	Channel width	200 nm
V_{dd}	Supply Voltage	1.2 V
T_{ox}	Gate oxide thickness	1.4 nm
N_{gate}	Polysilicon gate doping concentration	$2\times10^{+20}$ cm^{-3}
N_{dep}	Channel doping concentration	$2.5\times10^{+18}$ cm^{-3}
N_{sd}	Source/drain doping concentration	$2\times10^{+20}$ cm^{-3}
X_j	Junction depth	0.028 µm
N_{sub}	Substrate doping concentration	$2\times10^{+17}$ cm^{-3}
–	S/D electrode length	0.07 µm
–	S/D region to polygate	0.02 µm
–	Line-end Extension	50 nm
–	STI width	50 nm
–	STI depth	100 nm

B. Impacts of Narrow-width Related Edge Effects on Device Characteristics

Results of 2D and 3D device simulations are compared to examine the impacts of the narrow-width related edge effects on the device characteristics. Fig. 2 and Fig. 3 show the 2D and 3D NMOS device structures respectively. The 3D NMOS device is surrounded with an oxide material of 0.1 µm in depth and 0.05 µm in width. In the 2D simulation, the thickness simply represents a multiplier for the electrode currents and charges. The uniform current density across the gate width is equivalent with the absence of the narrow-width related edge effects.

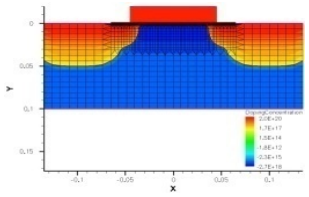


Fig. 2. A meshed 2D NMOS

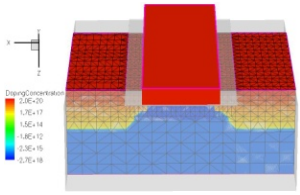


Fig. 3. A meshed 3D NMOS

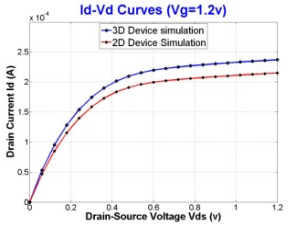


Fig. 4. Comparison of I_d-V_d curves at V_g=1.2 V of 2D and 3D device simulations.

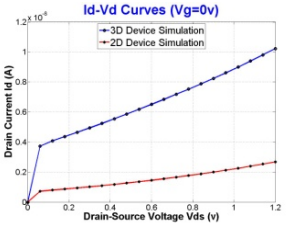


Fig. 5. Comparison of I_d-V_d curves at V_g=0 V of 2D and 3D device simulations.

For comparison, the thickness of the 2D device is set to the channel width of the 3D device, and their doping profiles are

equivalent. Fig. 4 and Fig. 5 show the I_d-V_d characteristics at V_g = 1.2 V (on state) and V_g = 0 V (off state) of the 2D and 3D devices with 200-nm channel width. The on-state drain current (I_{on}) of the 2D simulation is slightly less than that of the 3D simulation. This implies that the threshold voltage (V_{th}) deviation due to the narrow-width related edge effects on I_{on} is not substantial since I_{on} is not a very strong function of the threshold voltage (V_{th}). However, the off-state current (I_{off}) of the 3D simulation is up to three times larger than that of the 2D simulation because I_{off} is an exponential function of the V_{th}.

In TABLE II, the on-current (I_{on}) and off-current (I_{off}) of the 2D and 3D devices are listed for four different channel widths of 50 nm, 100 nm, 150 nm, and 200 nm. It shows that the narrower the device width, the larger the discrepancy between the 2D and 3D simulation results. This implies that the narrower-width devices suffer from more serious narrow-width related edge effects. This is because the boundary areas with the larger threshold voltage and current density variations occupy a larger fraction of the total gate width.

TABLE II
ON AND OFF CURRENTS OF 2D AND 3D DEVICES WITH DIFFERENT CHANNEL WIDTHS

	On Current			Off Current		
	3D	2D	Error	3D	2D	Error
W=50nm	68.9μA	53.8μA	-22%	4.86nA	0.67nA	-86%
W=100nm	129.2μA	107.6μA	-17%	7.10nA	1.34nA	-81%
W=150nm	181.7μA	161.3μA	-11%	8.53nA	2.01nA	-76%
W=200nm	237.1μA	215.1μA	-9%	10.23nA	2.69nA	-73%

C. Accuracy of Standard EGL Method

The pattern transfer fidelity of optical lithography is severely limited by electromagnetic (EM) wave diffraction in the sub-wavelength regime. Actual gate shape on the wafer can be significantly distorted from designed rectangular layout. To verify the accuracy of the standard EGL extraction method for the non-rectangular transistors, we construct a fictitious gate shape and channel region with rectangular slices of different lengths to imitate across-width gate length variation due to severe line-necking effects as shown in Fig. 6. Each slice is subject to location depend narrow-width related edge effects.

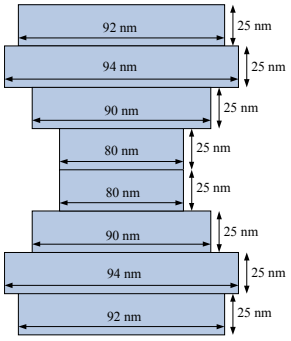


Fig. 6. Imitated non-rectangular gate shape.

The device with non-rectangular gate is simulated by the 3D device simulator. Each rectangular slice with its own channel length and width is also simulated by the 2D device simulator individually. This is equivalent with utilizing W_{big} in the standard EGL extraction approach, which effectively ensures uniform current density within each slice [9]. The currents of all the slices are then added up. We construct a current lookup table of various gate lengths from the 2D device simulations and extract the effective channel length whose current is closest to the sum of slice currents. In this case, the extracted on-state EGL ($L_{eff,on}$) and off-state EGL ($L_{eff,off}$) are 89 nm and 87 nm respectively. The device characteristics with both effective gate lengths are characterized by the 3D device simulation. Fig. 7 and Fig. 8 show the on-state and off-state I_d-V_d characteristics of the 3D non-rectangular gate device, the sum of the 2D-sliced rectangular devices, and the equivalent rectangular 3D device with the extracted EGLs. As shown in TABLE III, the characteristics of the equivalent rectangular device with the $L_{eff,on}$ well approximate those of the non-rectangular device at on state with the error less than 1%. However, the equivalent rectangular device with the $L_{eff,off}$ fails to match the characteristics of non-rectangular device at off state, and overestimates the leakage current by 19.6%.

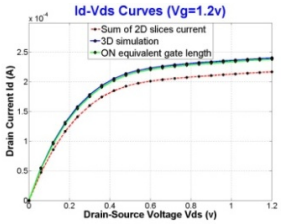


Fig. 7. Id-Vd (V_g=1.2 V) comparison of total current of 2D slices and 3D simulation.

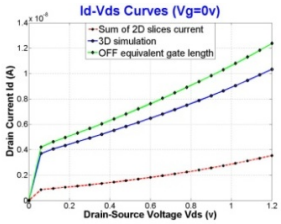


Fig. 8. Id-Vd (V_g=0 V) comparison of total current of 2D slices and 3D simulation.

TABLE III
ACCURACY OF EFFECTIVE GATE LENGTH EXTRACTION

	On-current	Off-current
3D with NRG	240.49 μA	10.34 nA
3D with EGL	238.46 μA	12.37 nA
Relative error	-0.84%	19.6%

III. ACCURATE LEAKAGE CURRENT ESTIMATION

A. Proposed Location-Dependent Weightings

From the previous discussions, we can find that the impacts of the narrow-width related edge effects on the off-state electrical characteristics are quite significant. The device with the standard EGL extraction method can not accurately estimate the sub-threshold characteristics of a real non-rectangular transistor, because location dependency is not taken into account. To improve the estimation accuracy of the leakage current (I_{off}) of the non-rectangular 3D transistors from the I_{off} information of the 2D slices, we can assume the existence of an effective location-dependent edge-effect weighting factor $W(\alpha_i)$ on the ideal 2D I_{off} current through each slice, according to its relative location on the channel. This concept is illustrated in Fig. 9. The I-V curve of a 3D device with a non-rectangular gate can be approximated by the sum of weighted I-V curves of n 2D slices as expressed in equation (1).

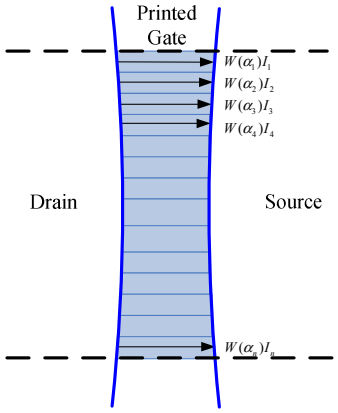


Fig. 9. Weighted 2D-sliced current.

$$I_{3D} \cong W(\alpha_1)I_{1,2D}(v) + W(\alpha_2)I_{2,2D}(v) + \cdots W(\alpha_n)I_{n,2D}(v) \tag{1}$$

where the non-rectangular gate is decomposed to n slices. $I_{i,2D}(v)$ stands for the I-V curve of the i^{th} slice and $W(\alpha_i)$ is the weighting factor of the i^{th} slice. We then take m points from each of the I-V curves. Equation (2), by expanding equation (1), is then

$$\begin{bmatrix} I(v_1) \\ I(v_2) \\ \vdots \\ I(v_m) \end{bmatrix}_{3D} \cong \begin{bmatrix} I_1(v_1) & I_2(v_1) & \cdots & I_n(v_1) \\ I_1(v_2) & I_2(v_2) & \cdots & I_n(v_2) \\ \vdots & \vdots & \cdots & \vdots \\ I_1(v_m) & I_2(v_m) & \cdots & I_n(v_m) \end{bmatrix}_{2D} \begin{bmatrix} W(\alpha_1) \\ W(\alpha_2) \\ \vdots \\ W(\alpha_n) \end{bmatrix} \tag{2}$$

To determine the best numerical values of the weighting factors $\{W(\alpha_i)\}$ by minimizing the estimation error in the least-square sense, a constrained linear least-squares optimization problem is formulated as follows.

$$\begin{aligned} \underset{w}{\text{minimize}} \quad & \frac{1}{2}\|Hw - y\|_2^2 \\ \text{subject to} \quad & w_l \le w \le w_u \end{aligned} \tag{3}$$

where $y \in \mathbf{R}^m$ is the target vector with the values of drain currents at different drain-source voltages of the 3D non-rectangular transistor from either 3D TCAD simulations or real silicon calibration data, $H \in \mathbf{R}^{m \times n}$ is the model matrix containing the values of the 2D-slice currents at different drain-source voltages and locations along the gate width, and w_l ,$w_u \in \mathbf{R}^n$ are the vector lower bound and vector upper bound of the weighting factor vector $w = [W(\alpha_1) \ \ldots \ W(\alpha_n)]^T$. This is a quadratic programming problem [3][15] where both the objective function and the constraint functions are convex, hence it can be solved very efficiently by interior-point methods. Due to the convex formulation, global optimum can be found without uncertainty of convergence.

B. Simulation Results

As a representative example of weighting factor extraction from silicon images and current measurements, eight 3D devices with different fictitious non-rectangular gate shapes shown in TABLE IV are simulated to generate eight I-V curves with V_g = 0 V. Each non-rectangular gate is constructed by ten rectangular slices with a fixed slice width of 20 nm and varying lengths of 82 nm, 86 nm, 90 nm, 94 nm, and 98 nm. The simulation results are incorporated with an expanded form of equation (2). Twenty samples are taken from each of the I-V curves. We constraint the weight factors by setting $0 \le w \le 10$. The lower bound is to impose non-negative weighting factors, while the upper bound is mainly to prevent over fitting to problematic data. By solving the quadratic programming problem, the extracted optimum weighting factors are as follows.

$$\begin{aligned} &[W(\alpha_1)\ W(\alpha_2)\ W(\alpha_3)\ W(\alpha_4)\ W(\alpha_5)\ W(\alpha_6)\ W(\alpha_7)\ W(\alpha_8)\ W(\alpha_9)\ W(\alpha_{10})]^T \\ &= [7.2682\ 4.1188\ 2.313\ 2.4057\ 2.2441\ 2.2441\ 2.4057\ 2.313\ 4.1188\ 7.2682]^T \end{aligned} \tag{4}$$

The results show that slices closer to the edges are weighted more. This is consistent with the physical phenomena that they have a stronger response to the fringing electric field and the current density is higher on both edges [10].

The extracted weighting factors are applied to the original eight non-rectangular gate transistors for self-validation. TABLE V summarizes the sum of the 2D-slice currents with and without the location-dependent weighting factors. The difference between the sum of the 2D-slice currents and 3D non-rectangular gate simulation result is about 40%~60%. However, after applying the extracted location-dependent weighting factors, the normalized mean-square error can be decreased to less than 0.7%. The weighted sum of the 2D-slice characteristics can approximate the characteristics of the 3D non-rectangular transistor quite well. An independent non-rectangular gate as shown in Fig. 10(a) is used to cross-validate the effectiveness of the weighting factor extraction. The extracted weighting factors are applied to this independent non-rectangular gate shape. The weighted sum of the 2D-slice currents and 3D simulation results are shown in Fig. 10(b). The difference between the 3D non-rectangular gate and the sum of the 2D-slice currents is 48.7%. With the weighting factors, the difference between the weighted sum of the 2D slices and the 3D non-rectangular device simulation is only 0.66%. This implies that the extracted weightings from limited TCAD or silicon calibration data may be applied to any type of actual non-rectangular gate shape encountered.

Finally, the extracted location-dependent weighting factors are utilized to obtain the off-state EGL ($L_{eff,off}$). The independent non-rectangular gate shown in Fig. 10(a) is used again. The weighted sum of off-state currents of the 2D slices is compared to the off-state current lookup table of varying gate length. The off-state effective gate length with and without the weighting factors are then extracted by interpolation. The standard off-state EGL for this non-rectangular gate is 87 nm. The off-state EGL involving the location dependent weighting factors is 88 nm. The leakage current estimations of these two effective gate length methods are listed in TABLE VI. The standard EGL extraction method leads to 15.9% overestimation of the leakage current. With the new EGL extraction method, the error can be decreased to 7.4% in this case.

TABLE IV
EIGHT TYPES OF NON-RECTANGULAR GATE SHAPES

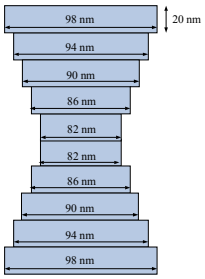
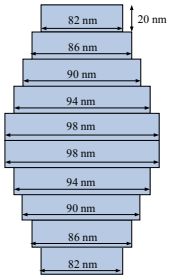
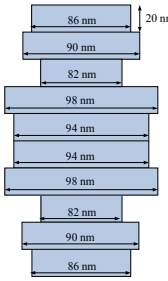
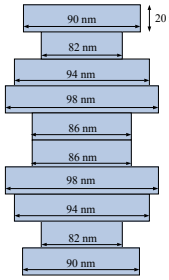
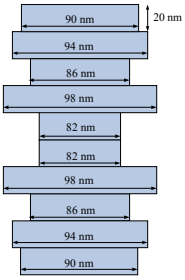
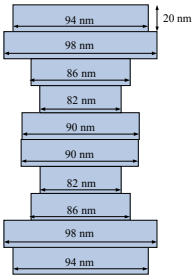
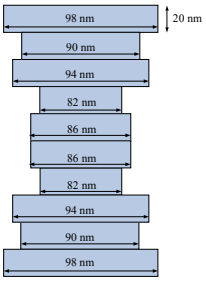
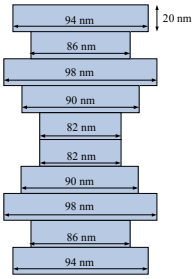
Eight different non-rectangular gate shapes			
Type 1	Type 2	Type 3	Type 4
			
Type 5	Type 6	Type 7	Type 8
			

TABLE V
SELF-VALIDATION FOR EXTRACTED WEIGHTINGS

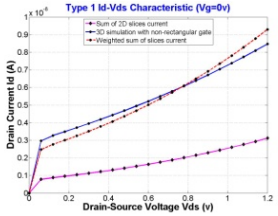
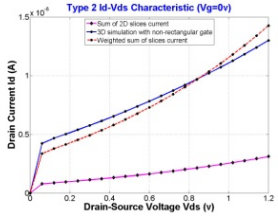
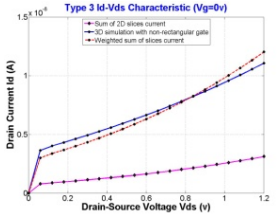
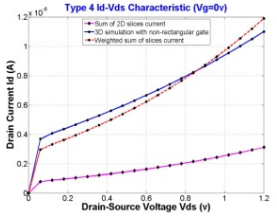
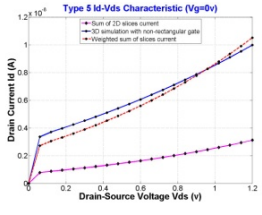
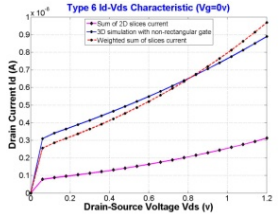
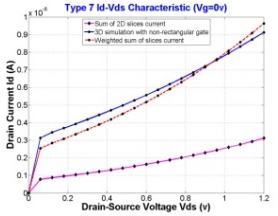
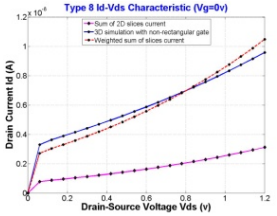
Error of the sum of 2D slices and the weighted sum			
 Error of the sum of 2D slices=44.4% Error of the weighted sum=0.52%	 Error of the sum of 2D slices=60.7% Error of the weighted sum=0.66%	 Error of the sum of 2D slices=54.8% Error of the weighted sum=0.49%	 Error of the sum of 2D slices=54.8% Error of the weighted sum=0.57%
 Error of the sum of 2D slices=60.0% Error of the weighted sum=0.50%	 Error of the sum of 2D slices=46.6% Error of the weighted sum=0.52%	 Error of the sum of 2D slices=47.4% Error of the weighted sum=0.48%	 Error of the sum of 2D slices=49.6% Error of the weighted sum=0.54%

TABLE VI
COMPARISON OF LEAKAGE CURRENT ESTIMATION WITH DIFFERENT EGLS

	Leakage current	Error
3D NRG Device Simulation	10.7 nA	–
3D with Standard EGL	12.4 nA	15.9%
3D EGL with weightings	11.5 nA	7.4%

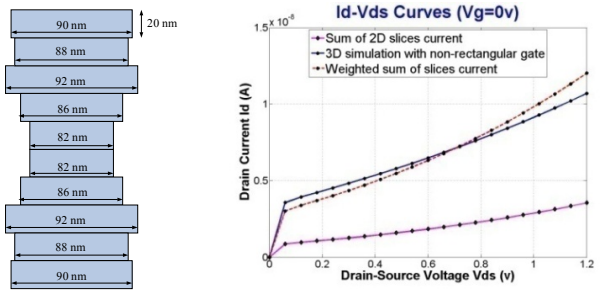


Fig. 10. (a) Non-rectangular gate shape for cross-validation. (b) I_d-V_d (V_g=0V) characteristics of 2D-sliced sum, 2D-weighted sum, and 3D simulation.

IV. Conclusion and Future Work

We have utilized TCAD device simulations to estimate impacts of narrow-width related edge effects on device characteristics. These edge effects result in appreciable variation of off-state current (I_{off}) and the variation becomes more serious as the channel width decreases. The sum of the off-state current of flat slices cannot approximate the off-state current of a non-rectangular transistor well. The standard EGL extraction method without considering the location dependency of the edge effects can lead to inaccurate estimation of leakage current. A new location-dependent-weighting approach has been proposed to compensate the leakage current variation due to the edge effects. The extraction algorithm is based on convex programming such that a globally optimal solution of weighting factors can be solved very efficiently. Programming and automation can be done in a straightforward way and application is intuitive. The preliminary results indicate that it can be a promising method for improving the accuracy of post-lithography static power analysis.

Several interesting situations should be considered to further validate the proposed method. Leakage current at different levels of the gate voltage should be analyzed for a more detailed static power analysis. Clearly, a sufficiently large number of gate shapes from post-OPC simulation or silicon images should be included for realistic EGL extraction.

There can be several immediate extensions and applications of the proposed method. Depending on different preferred usages of the method, one may extract independent weighting factors for any devices with different widths, or to develop a device-independent set of weighting factors by including current data over any devices. When a unique EGL for both the on and off states is preferred, one may include the current data of the on and off states. The accuracy tradeoff between both states can be adjusted by assigning additional cost weighting factors such that one solves:

$$\begin{aligned} \underset{w}{\text{minimize}} \quad & \frac{1}{2}\|FHw - y\|_2^2 \\ \text{subject to} \quad & w_l \le w \le w_u \end{aligned} \tag{5}$$

where F is a diagonal matrix with diagonal elements being the cost weighting factors. Furthermore, when transistor behavior at arbitrary gate voltages needs to be analyzed, the proposed location-dependent-weighting-factor method can be combined with the unified non-rectangular device model card method [12]. The model card is created based on I-V properties of the device. It can be added to each transistor with any available device model to modify the drain-source current according to the biasing condition and the non-rectangular gate shape. This approach does not need to evaluate the equivalent gate length. Accurate coherent circuit simulations can be done while the narrow-width related edge effects are not neglected.

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